HITACHI MICROCOMPUTER SYSTEM

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER & DRIVER LCD-Ⅱ (HD44780) USER'S MANUAL

—PRELIMINARY—

40-1-11

HITACHI

HITACHI MICROCOMPUTER SYSTEM

DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER & DRIVER LCD-Ⅱ (HD44780) USER'S MANUAL

—PRELIMINARY—

HITACHI

40-1-11

MARCH, 1981 40-1-11

When using this manual, the reader should keep the following in mind:

1. This manual may, wholly or partially, be subject to changes without notice.

2. All rights reserved: No one is permitted to reproduce or duplicate, in any form, the whole or a part of this manual without Hitachi's permission.

3. Hitachi will not be responsible for any damage to the user that may result from accidents or any other reasons during operation of his unit according to this manual.

4. This manual neither ensures the enforcement of any industrial properties or other rights, nor sanctions the enforcement right thereof.

MARCH, 1981

PREFACE

The LCD-II (HD44780) is a dot matrix liquid crystal display controller& driver LSI that displays alphanumerics, kana charactors and symbols.

It drives dot matrix liquid crystal display under 4-bit or 8-bit microcomputer control.

All functions needed for dot matrix liquid crystal display drive are internally provided on one chip.

The user can complete dot matrix liquid crystal display systems with less number of chips by using the LCD-II (HD44780).

CONTENTS

1. Outline 1

2. Features 2

3. Logical Structure and Function 3

3.1 Symbol Diagram 3

3.2 Pin Assignment and Dimentional Outline 4

3.3 Terminal Function 5

3.4 Block Diagram 6

3.5 Function of Each Block 7

3.6 Interfacing to MPU 16

3.7 Reset Function 17

4. Instruction 18

4.1 Outline 18

4.2 Description of Details 20

5. Electrical Characteristics 23

5.1 Absolute Maximum Ratings 23

5.2 Electrical Characteristics 24

5.3 Timing Characteristics 27

6. How to Use HD44780 29

6.1 Interface to 8-bit MPU 29

6.2 Interface to Liquid Crystal Display 31

6.3 Power Supply for Liquid Crystal Display Drive 33

6.4 Liquid Crystal Display Drive Waveform 36

6.5 Connection with Driver LSI HD44100 38

6.6 Correspondence Example of Instructions and Display 41

7. Appendix 45

1. Outline

The LCD-II (type No. HD44780, hereinafter called HD44780) is a dot matrix liquid crystal display controller & driver LSI for display of alphanumerics, kana characters and symbols. It memorizes character codes (8 bits/character) sent from microcomputers or microprocessors (hereinafter called MPU) into display data RAM (DD RAM, 80 bytes=640 bits, 80 character size), converts them to dot matrix character patterns of either 5×7 dots or 5×10 dots, which are then sent to the internal liquid crystal display driver. Since the HD44780 has an internal 16-common signal driver and 40-segment signal driver, one HD44780 can display up to 16 characters (in the case of 1 character being 5×7 dots, 1/16 duty). If a driver LSI HD44100 is externally connected to the HD44780, up to 80 characters can be displayed.

The HD44780 is internally equipped with character generator ROM (CG ROM) that generates 160 types of alphanumerics, kana characters and symbols (character font 5×7 dots, in conformity to JIS) and 32 types of special characters (Greek letters and others, character font 5×10 dots). Further, it is equipped with character generator RAM (CG RAM, 64 bytes=512 bits) in the size of 8 characters if with character font of 5×7 dots, or size of 4 characters if with 5×10 dots. CG RAM can be programmed for each application. The above feature offers a lot of convenience in actual use. The user can specify any character pattern for character generator ROM. For details, refer to "The LCD-II (HD44780) Breadboard User's Manual".

To designate character display position, write an instruction into the instruction register from MPU via data bus and then write a character code into the data register via data bus. Since the HD44780 has a function of automatically shifting character display positions after character codes are written, character displays at continuous positions from the next operation on is possible, by writing only character codes. Also, since the HD44780 has the shift function of the entire display, display input from either left or right is possible.

Since both of the display data RAM and character generator RAM can be read from MPU, whatever part that is not used for display can be used as general data RAM.

The HD44780 is a CMOS LSI of 80-pin plastic flat package. It can transfer data in 4-bit-2-operation or 8-bit-1-operation, allowing interface to MPU of either 4 or 8 bit. When combined with a CMOS MPU, the user can develop portable battery drive equipment utilizing low power consumption of the liquid crystal display.

2. Features

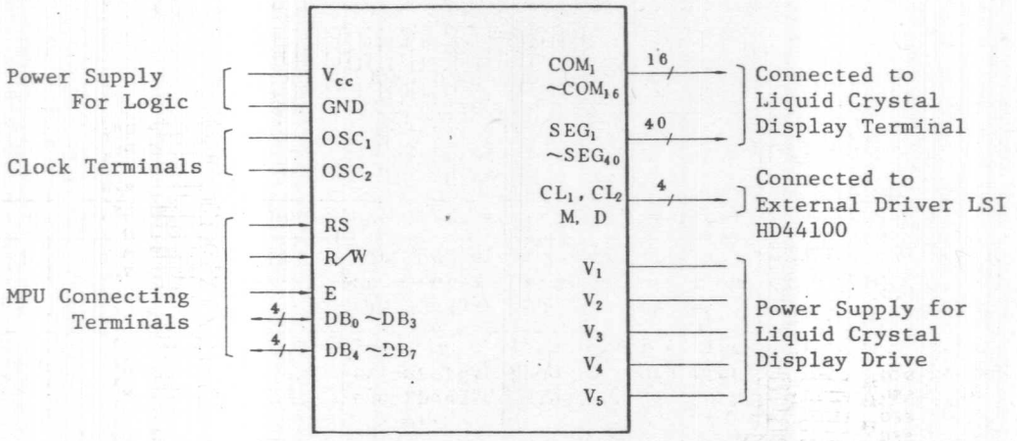
- 5×7 and 5×10 dot matrix liquid crystal display controller driver
- Capable of interfacing to 4-bit or 8-bit MPU.
- Display data RAM ..... 80×8 bits (80 characters, max.)
- Character generator ROM .....
  - Alphanumerics and symbols: 96 types; A～Z, a～z, etc. (5×7 dot character font)
  - Kana characters and symbols: 64 types; ｱ～ﾝ, 「 」, etc. (5×7 dot character font)
  - Special characters: 32 types; α, β, Ω, etc. (5×10 dot character font)
- Character generator RAM .....
  - Programmable: 8 types of 5×7 dot character font, or
    4 types of 5×10 dot character font
- Both of display data and character generator RAMs can be read from MPU.
- Internal liquid crystal display driver ..... 16 common signal drivers
  40 segment signal drivers
- Duty factor selection (selected by programs) .....
  - 1/8 duty: 1 line of 5×7 dots + cursor
  - 1/11 duty: 1 line of 5×10 dots + cursor
  - 1/16 duty: 2 lines of 5×7 dots + cursor
- Maximum number of display characters

No.of Display Lines	Duty Factor	Extention	HD44780	HD44100	No.of Display Characters
1-line display	1/8 1/11 duty	Not provided	1 pc.	-----	8 characters×1 line
		Provided	1 pc.	9 pcs. (8 characters/pc.)	80 characters×1 line
2-line display	1/16 duty	Not provided	1 pc.	-----	8 characters×2 lines
		Provided	1 pc.	4 pcs. (8 characters×2 lines/pc.)	40 characters×2 lines

- Wide range of instruction function
  Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF,
  Display character blink, Cursor shift, Display shift
- Internal automatic reset circuit at power ON.
- Internal oscillation circuit (with an external resistor or ceramic filter)
  (External clock operation is possible.)
- CMOS process
- Logic power supply; A single+5V (excluding power for liquid crystal display drive)
- Operation temperature range; -20～+75°C
  (Device for -40～+85°C is available upon request)
- 80-pin plastic flat package (FP-80)

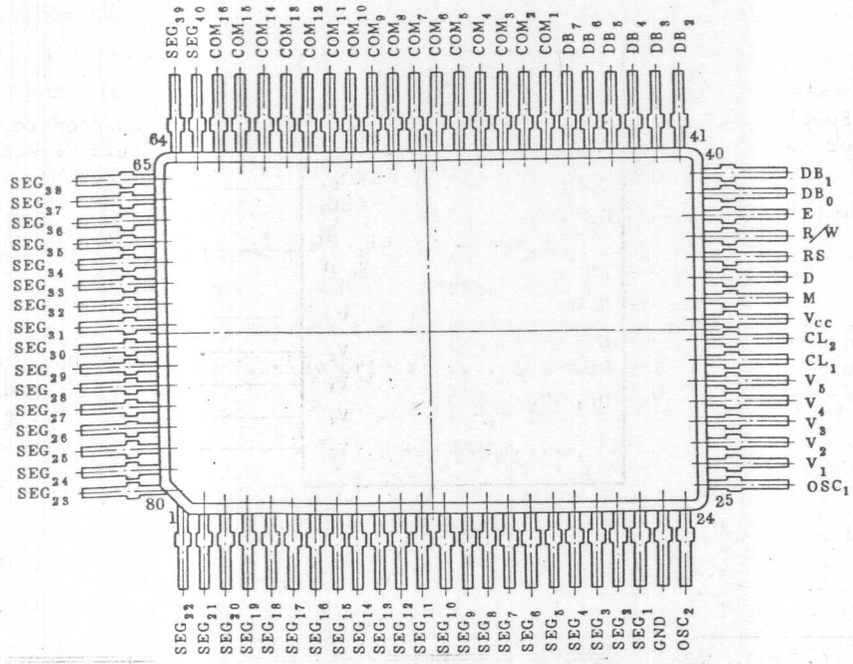
3. Logical Structure and Function

3.1 Symbol Diagram

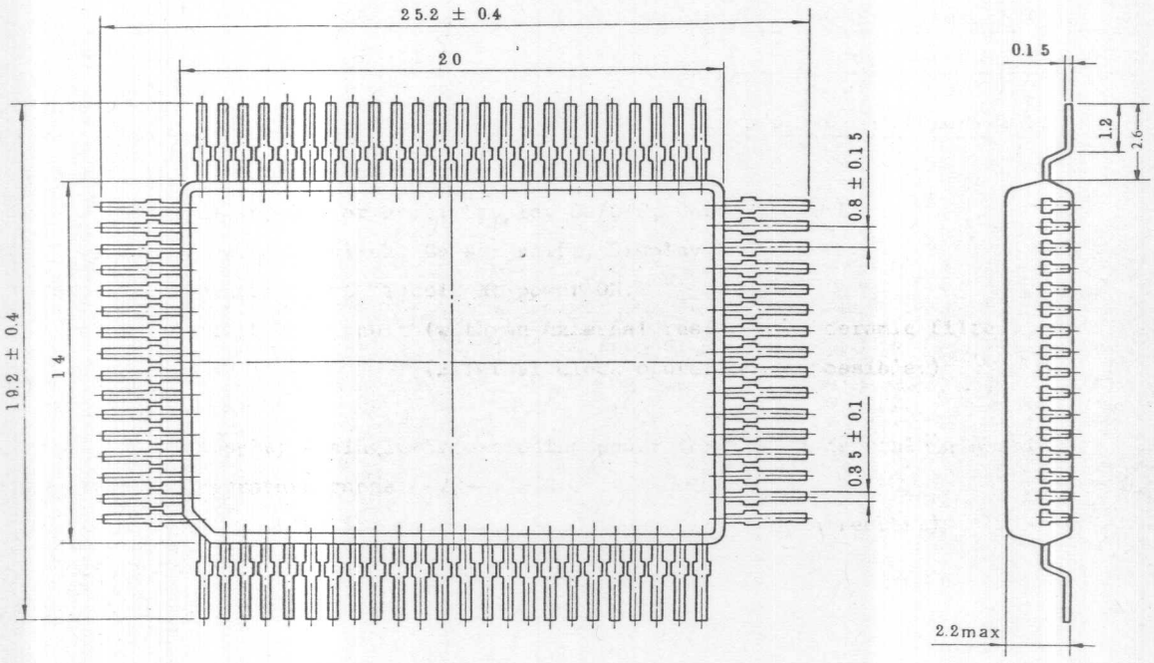


3.2 Pin Assignment and Dimentional Outline

(1) Pin Assignment



(2) Package Dimentional Outline (80 Pin Plastic Flat Package)



(FP-80)

(Unit:mm)

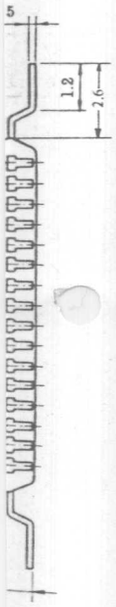
3.3 Te

Signal name
RS
R/W
E
DB4 ~ DB7
DB0 ~ DB3
CL1
CL2
M
D
COM1 ~ COM16
SEG1 ~ SEG40
V1 ~ V5
Vcc, GN
OSC1, OSC2

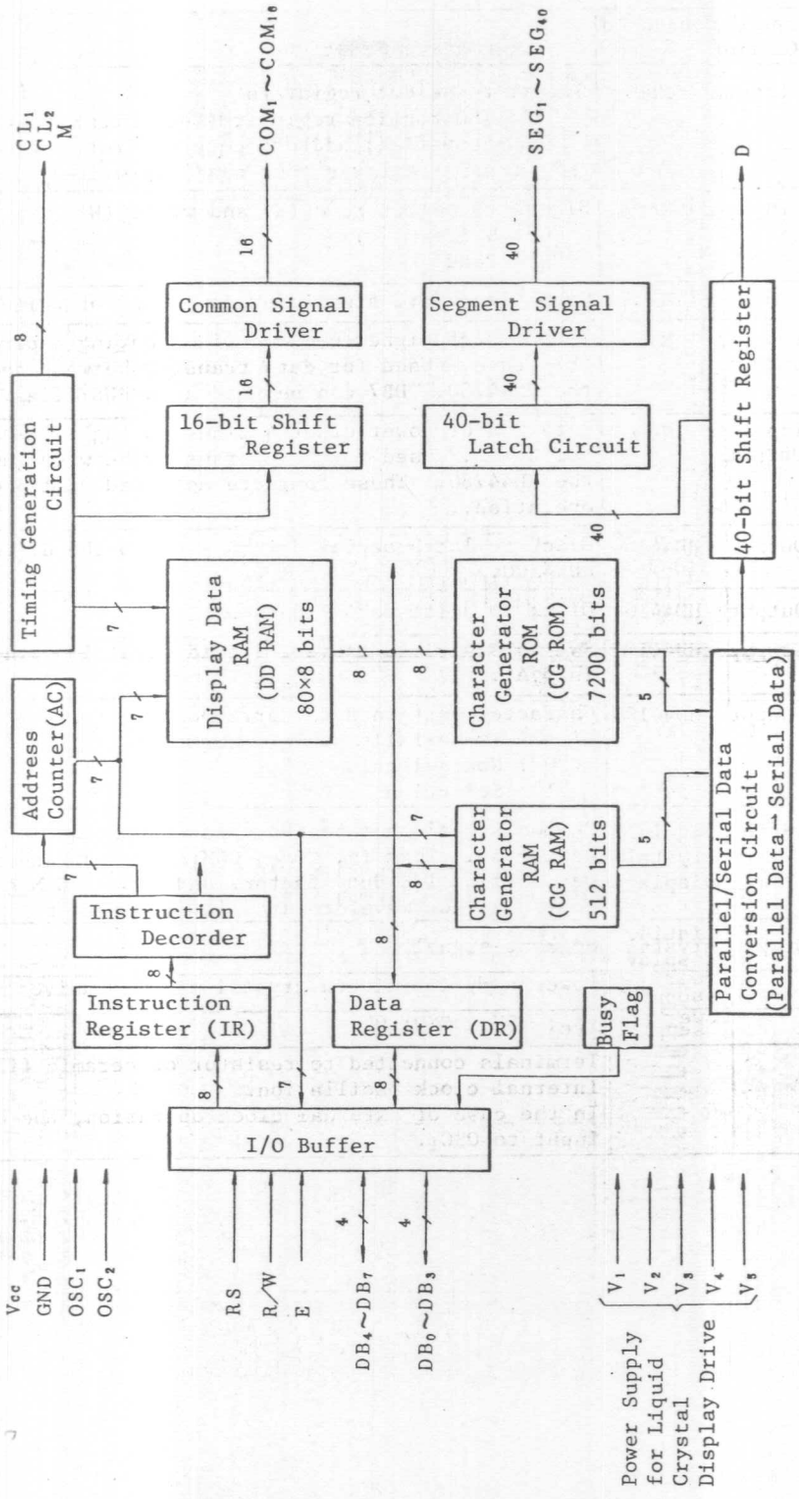
3.3 Terminal Function

Table 3.1 Functional Description of the Terminals

Signal name	No.of lines	Input/ Output	Connected to	Function
RS	1	Input	MPU	Signal to select registers "0": Instruction register (for write) Busy flag; address counter (for read) "1": Data register (for read and write)
R/W	1	Input	MPU	Signal to select read (R) and write (W) "0": Write "1": Read
E	1	Input	MPU	Operation start signal for data read or write
DB_4 ~ DB_7	4	Input/ Output	MPU	Data bus of higher order 4 lines having bidirectional tri-state. Used for data transfer between the MPU and the HD44780. DB7 can be used as a BUSY flag.
DB_0 ~ DB_3	4	Input/ Output	MPU	Data bus of lower order 4 lines having bidirectional tri-state. Used for data transfer between the MPU and the HD44780. These four are not used during 4-bit operation.
CL_1	1	Output	HD44100	Clock to latch serial data D sent to the driver LSI HD44100.
CL_2	1	Output	HD44100	Clock to shift serial data D.
M	1	Output	HD44100	Switch signal to convert liquid crystal drive waveform into AC.
D	1	Output	HD44100	Character pattern data corresponding to each common signal is serially sent in sequence. "0": Non selection "1": Selection
COM_1 ~ COM_{16}	16	Output	Liquid crystal display	Common signal that are not used are made to non-selection waveforms. That is, COM_9 ~ COM_{16} are in non-selection waveform at 1/8 duty factor, and COM_{12} ~ COM_{16} are in non-selection waveform at 1/11 duty factor.
SEG_1 ~ SEG_{40}	40	Output	Liquid crystal display	Segment signal
V_1 ~ V_5	5		Power supply	Power supply for liquid crystal display drive
V_{cc}, GND	2		Power supply	V_{cc}; +5V, GND; 0V
OSC_1, OSC_2	2			Terminals connected to resistor or ceramic filter for internal clock oscillation. In the case of external clock operation, the clock is input to OSC_1.



3.4 Block Diagram (The Internal of HD44780)



3.5 Function of Each Block

(1) Register

The HD44780 has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR).

IR stores instruction codes such as display clear and cursor shift, and address information of display data RAM (DD RAM) and character generator RAM (CG RAM). IR can be written from MPU but not read by MPU.

DR temporarily stores data to be written into the DD RAM or the CG RAM. Data written into DR from MPU is automatically sent to the DD RAM or the CG RAM as an internal operation. DR is also used for data storage when reading data from the DD RAM or the CG RAM. When address information is written into IR, data is transferred to DR from the DD RAM or the CG RAM as an internal operation. Then, data transfer to the MPU is completed by the MPU reading DR. After the MPU reads DR, data of the DD RAM or the CG RAM at the next address is sent to DR for the next read from the MPU.

Register selector (RS) signals select these two registers.

Table 3.2 Register selection

RS	R/W	Operation
0	0	IR write as internal operations (Display clear, etc.)
0	1	Read of a BUSY flag (DB_7) and address counter ($DB_0 \sim DB_6$)
1	0	DR write as internal operations (DR to DD or CG RAM)
1	1	DR read as internal operations (DD or CG RAM to DR)

(2) Busy flag (BF)

When the Busy flag is "1", the HD44780 is in the internal operation mode, and the next instruction is not accepted at this time. As shown in Table 3.2, the Busy flag is output to DB_7 when RS=0 and R/W=1. The next instruction must be written after checking that the Busy flag is "0".

(3) Address counter (AC)

The address counter (AC) assigns address to DD and CG RAMs. When as instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.

After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by -1). AC contents are output to $DB_0 \sim DB_6$ when RS=0 and R/W=1, as shown in Table 3.2.

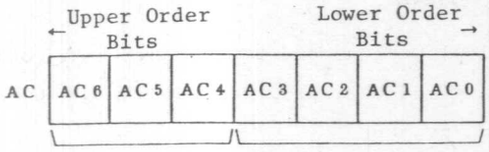
(4) Display data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80×8 bits, which can contain 80 characters. The display data RAM (DD RAM) that is not used for display can be used as general data RAM.

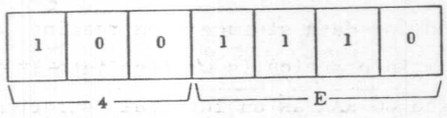
Relation between DD RAM addresses and positions on the liquid crystal display

is as shown below.

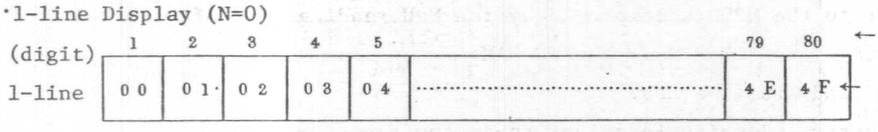
The DD RAM address (A_{DD}) which is set in the Address Counter (AC) is represented in hexadecimal.



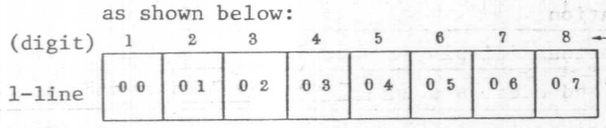
(Example) DD RAM address "4E"



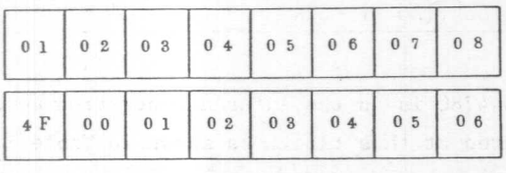
·1-line Display (N=0)



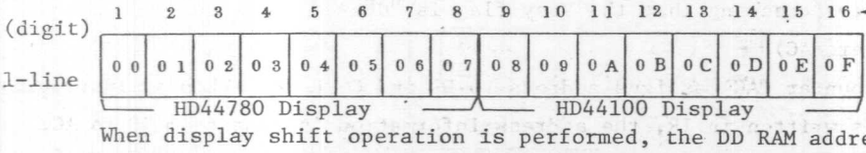
(a) When number of display characters is less than 80, the display starts from the head position. For example, 8 characters using 1 HD44780 are displayed as shown below:



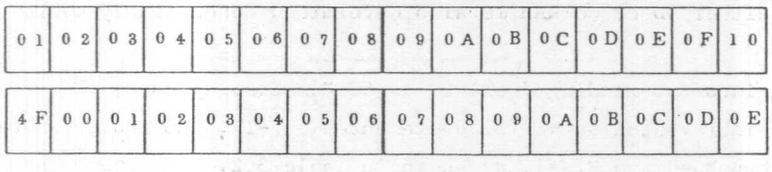
When display shift operation is performed, the DD RAM address moves as follows:



(b) 16-character display using an HD44780 and an HD44100 is as shown below:



When display shift operation is performed, the DD RAM address moves as follows:



(c) Relation between display position and the DD RAM address when number of display digits is increased by using one HD44780 and two or more HD44100's can be considered extension of (b).

Since 8 digits can be increased for each additional HD44100, display of up to 80 digits is possible by connecting 9 HD44100's externally.

・2-line Display (N=1)

(digit)	1	2	3	4	5	.....	39	40	← Display Position
1-line	00	01	02	03	04	.....	26	27	← DD RAM Address
2-line	40	41	42	43	44	.....	66	67	

(a) When number of display characters is less than 40 characters × 2 lines, 2 lines starting from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD44780 is used, 8 characters × 2 lines are displayed as follows:

(digit)	1	2	3	4	5	6	7	8	← Display Position
1-line	00	01	02	03	04	05	06	07	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	

When display shift is performed, the DD RAM address moves as follows:

	01	02	03	04	05	06	07	08
(Left Shift Display)	41	42	43	44	45	46	47	48

	27	00	01	02	03	04	05	06
(Right Shift Display)	67	40	41	42	43	44	45	46

(b) 16 characters × 2 lines are displayed as follows when an HD44780 and an HD44100 are used:

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

HD44780 Display | HD44100 Display

When display shift is performed, the DD RAM address moves as follows:

	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	(Left Shift Display)
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	

	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	(Right Shift Display)
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

(c) Relation between display position and DD RAM address when number of display digits is increased by using one HD44780 and two or more HD44100's, can be considered extension of (b).

Since display columns are increased by 8 digits× 2 lines for each additional HD44100, display of up to 40 digits× 2 lines is possible by connecting 4 HD44780's externally.

(5) Character Generator ROM (CG ROM)

The character generator ROM generates character patterns of 5×7 dots or 5×10 dots from 8-bit character codes. It can generates 160 types of 5×7 dot character patterns and 32 types of 5×10 dot character patterns. Table 3.3 and 3.4 show correspondence between character codes and character patterns. Also, the user defined character patterns are available by mask-programming ROM. For details, refer to "The LCD-II (HD44780) Breadboard User's Manual".

(6) Character Generator RAM (CG RAM)

The character generator RAM is the RAM with which the user can rewrite character patterns by program. In the case of 5×7 dots, 8 types of character patterns can be written and in the case of 5×10 dots 4 types. Write the character codes listed in the left edges of Table 3.3 and 3.4 to display character patterns stored in CG RAM.

Table 3.5 shows relation between CG RAM addresses and data and display patterns.

As shown in Table 3.5, area that is not used for display can be used as general data RAM.

Table 3.3 Correspondence between Character Codes and Character Pattern

Higher / Lower 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
××××0000	CG RAM (1)												
××××0001	(2)												
××××0010	(3)												
××××0011	(4)												
××××0100	(5)												
××××0101	(6)												
××××0110	(7)												
××××0111	(8)												
××××1000	(1)												
××××1001	(2)												
××××1010	(3)												
××××1011	(4)												
××××1100	(5)												
××××1101	(6)												
××××1110	(7)												
××××1111	(8)												

Table 3.4 Correspondence between Character Codes and Character

Lower 4bit \ Higher 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
××××0000	CG RAM (1)		0	@	P	¥	p		—	タ	ミ	α	p
××××0001	(2)	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
××××0010	(3)	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
××××0011	(4)	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
××××0100	(5)	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
××××0101	(6)	%	5	E	U	e	u	・	オ	ナ	ユ	σ	ü
××××0110	(7)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
××××0111	(8)	'	7	G	W	g	w	ァ	キ	ヌ	ラ	g	π
××××1000	(1)	(	8	H	X	h	x	ィ	ク	ネ	リ	√	x̄
××××1001	(2)	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	-1	y
××××1010	(3)	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	千
××××1011	(4)	+	;	K	[	k	{	ォ	サ	ヒ	ロ	x	万
××××1100	(5)	,	<	L	¥	l	|	ャ	シ	フ	ワ	¢	円
××××1101	(6)	-	=	M	]	m	}	ュ	ス	ヘ	ン	£	÷
××××1110	(7)	.	>	N	^	n	→	ョ	セ	ホ	゜	n̄	
××××1111	(8)	/	?	O	_	o	←	ッ	ソ	マ	°	ö	

Table 3.5 Relation between CG RAM Addresses and Character Codes (DD RAM) and Character Patterns (CG RAM Data)

(a) For 5×7 dot character patterns

Character Codes (DD RAM Data)	CG RAM Address	Character Patterns (CG RAM Data)	
7 6 5 4 3 2 1 0 ←Higher Order Bits Lower Order Bits→	5 4 3 2 1 0 ←Higher Order Bits Lower Order Bits→	7 6 5 4 3 2 1 0 ←Higher Order Bits Lower Order Bits→	
0 0 0 0 ∗ 0 0 0	0 0 0 0 0 0	∗ ∗ ∗ 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 ∗ ∗ ∗ 0 0 0 0 0	Character Pattern Example (1) Cursor ← Position
0 0 0 0 ∗ 0 0 1	0 0 1 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	∗ ∗ ∗ 1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 ∗ ∗ ∗ 0 0 0 0 0	Character Pattern Example (2)
	0 0 0 0 0 1	∗ ∗ ∗	
0 0 0 0 ∗ 1 1 1	1 1 1 1 0 0 1 0 1 1 1 0 1 1 1	∗ ∗ ∗	∗ Don't Care

Note 1: Character code bits 0～2 correspond to CG RAM address bits 3～5 (3 bits:8 types).

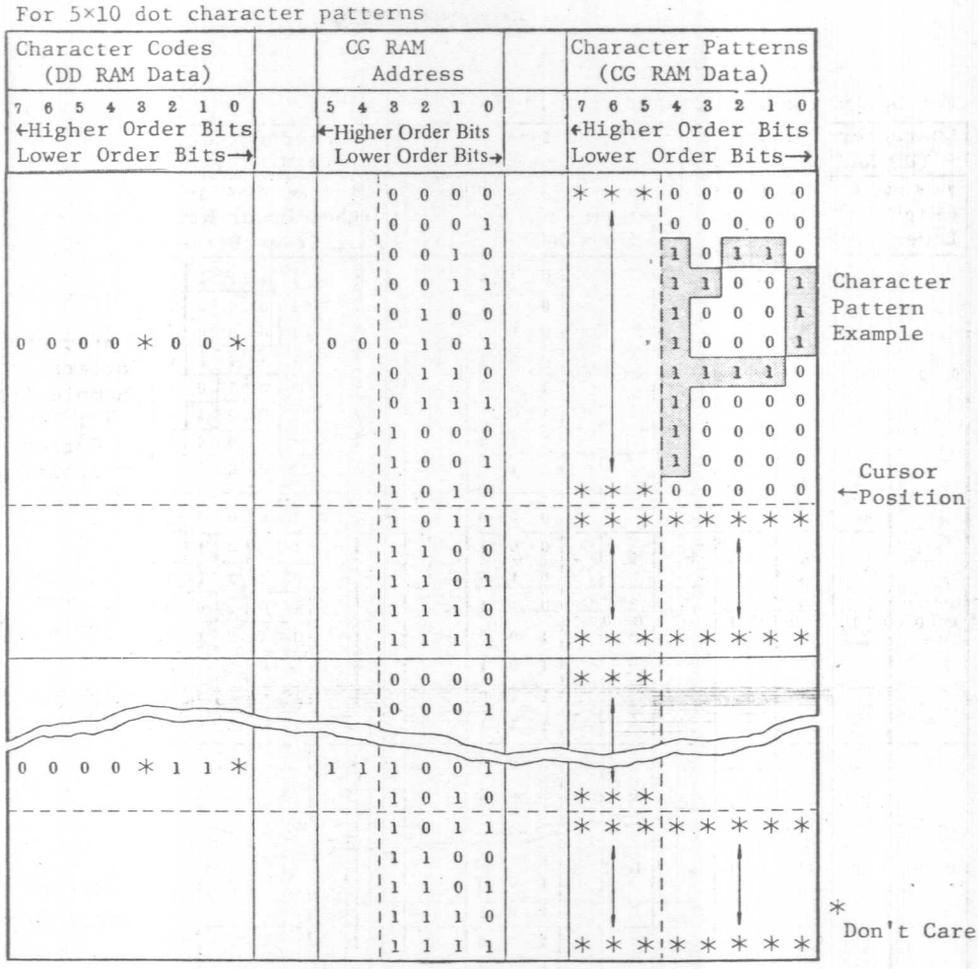
2: CG RAM address bits 0～2 designate character pattern line position. The 8th line is the cursor position and display is performed in logical OR with cursor.

3: Character pattern row positions correspond to CG RAM data bits 0～4, as shown in the figure (Bit 4 being at the left end). Since CG RAM data bits 5～7 are not used for display, they can be used as general data RAM.

4: As shown in Table 3.3 and 3.4, CG RAM character patterns are selected when character code bits 4～7 are all "0". However, since character code bit 3 is an don't care bit, "R" display in the chatacter pattern example, for example, are selected by character code "00"(hexadecimal) or "08"(hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(b) For 5×10 dot character patterns



Note 1: Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits:4 types).

2: CG RAM address bits 0 ~ 3 designate character pattern line position. The 11th line is the cursor position and display is performed in logical OR with cursor.
Since the 12th ~ 16th lines are not used for display, they can be used as general data RAM.

3: Character pattern row positions are the same as the positions for 5×7 dot character patterns.

4: CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 0 and 3 are don't care bits, "P" display in the character pattern example, for example, are selected by character code "00", "01", "08" and "09"(hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(7) Timing Generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, the CG ROM and the CG RAM. RAM read timings needed for display and internal operation timings by MPU accesses are separately generated so that they do not interfere with each other. Therefore, there will be no undesirable influence like flickering in areas other than display area of, for example, when writing data to the DD RAM.

This circuit also generates timing signals to operate the externally connected driver LSI HD44100.

(8) Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When a character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, and other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the driver LSI HD44100 (see Fig. 6.12). Character pattern data is serially sent through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver to generate drive waveform outputs.

The serial data is sent to the HD44100 externally connected in cascade and used for extension of number of display digits.

Send of serial data starts always at the display data character pattern corresponding to the last address of the display data RAM (DD RAM), and since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD44780 drives the head display and the rest displays corresponding to latter addresses are added with each additional HD44100.

3.6 Interfacing to MPU

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of $DB_4 \sim DB7$ and $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of $DB_0 \sim DB_3$ when interface data is 8 bits long).

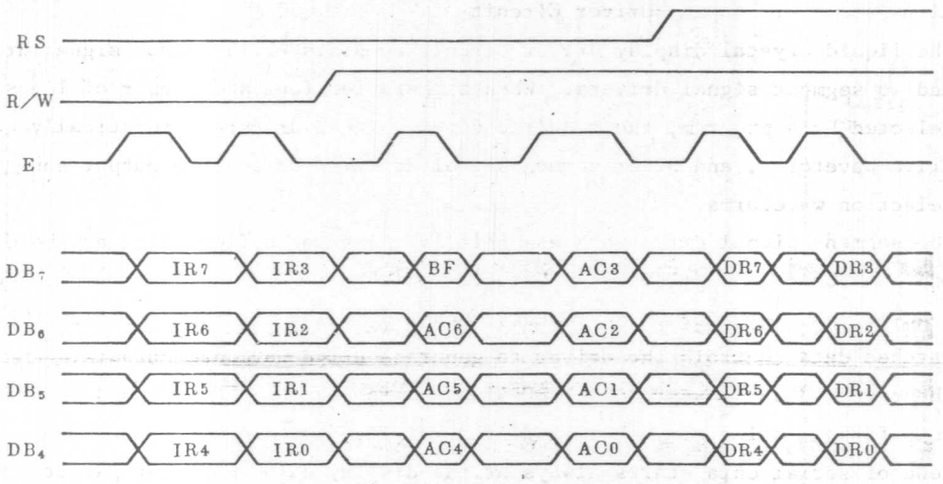


Fig. 3.1 4-bit Data Transfer Example

(2) When interface data is 8 bits long, data is transferred using 8 data buses of $DB_0 \sim DB7$.

3.7 Reset Function

The HD44780 automatically performs initialization (reset) when power is turned on (using internal reset circuit). The following instructions are executed in initialization:

(1) Clear display

The busy flag is kept in the busy state (BF=1) until initialization ends. The time is 15ms.

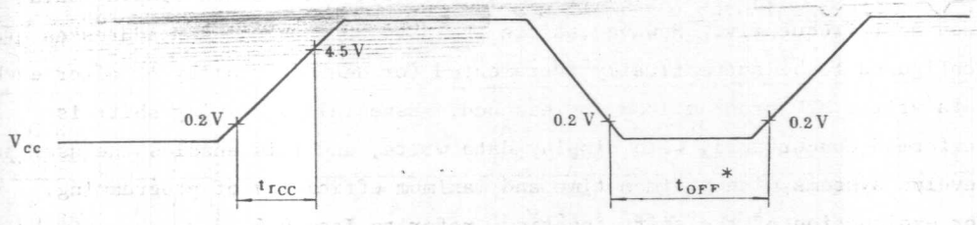
(2) Function set..... DL=1 : 8 bits long interface data
N =0 : 1-line display
F =0 : 5×7 dot character font

(3) Display ON/OFF control ..... D =0 : Display OFF
C =0 : Cursor OFF
B =0 : Blink OFF

(4) Entry mode set..... I/O=1 : +1 (increment)
S =0 : No shift

(5) DD RAM is selected

Because initialization may not be performed completely depending on the rise time of the power supply when it is turned on, pay attention to the following time relationship.



$0.1\,ms \leqq t_{rcc} \leqq 10\,ms$ $\quad t_{OFF} \geqq 1\,ms$

t_{OFF} stipulates the time of power OFF for power supply instantaneous dip or when power supply repeats ON and OFF.

Note: When the above power supply condition is not satisfied, the internal reset circuit does not operate normally. In this case, perform the needed initialization by sending instructions from MPU after turning the power ON. When initialization by the internal reset circuit is not performed normally, whether the interface data is 4 bits long or 8 bits long is not clear. Therefore, designate 8-bit data length by sending the function set instruction twice and then perform the required initialization. (See Chapter 4, Instruction.)

RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	*	*	*	*
0	0	0	0	1	1	*	*	*	*

When this instruction is sent, the HD44780 enters the 8-bit data length mode without fall.

4. Instruction

4.1 Outline

Two registers of the HD44780, the Instruction Register (IR) and the Data Register (DR) only can be controlled by MPU directly. Control information is temporarily stored in these registers, prior to internal operation start, to allow interface to various types of MPUs which operate in different speeds from HD44780 internal operation or to allow interface to peripheral control ICs. The HD44780 internal operation is determined by signals sent from the MPU, these signals including register selection signals (RS), read/write signals (R/W) and data bus signals (DB_0 - DB_7), are called instructions in this paragraph. Table 4.1 shows the instructions and the execution time of the instructions. Details are explained in the following sections. The instructions can be divided into the following 4 types:

(1) Instructions that designate the HD44780 functions such as display format, data length, etc.

(2) Instructions that give internal RAM addresses.

(3) Instructions that perform data transfer with internal RAM.

(4) Other instructions

In the normal use, instructions of category (3), which sends display data, is used most frequently. However, since the HD44780 internal RAM addresses are configured to be automatically incremented (or decremented) by +1 after each data write, MPU program load is lessened. Especially, display shift is performed concurrently with display data write, and this enables the user to develop systems with minimum time and maximum efficiency of programming. For explanation of the shift function, refer to Item 6.6.

When an instruction is being executed (during internal operation), no instruction other than Busy flag/address read instructions is executed. Because the Busy flag is set to "1" while an instruction is being executed, this must be checked prior to sending an instruction from the MPU.

Table 4.1 Instructions

Instruction	Code										Description	Execution Time (when fcp or fosc is 250 KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	82μs~1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	40μs~1.6ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents.	40μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL) number of display lines (L) and character font (F).	40μs
Set CG RAM Address	0	0	0	1	A_{CG}						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40μs
Set DD RAM Address	0	0	1	A_{DD}							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	40μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40μs
Read Data to CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40μs
	I/D=1: Increment I/D=0: Decrement S =1: Accompanies display shift. S/C=1: Display shift S/C=0: Cursor move R/L=1: Shift to the right. R/L=0: Shifts to the left. DL=1: 8 bits, DL=0: 4 bits N=1: 2 lines, N=0: 1 line F=1: 5×10 dots, F=0: 5×7 dots BF=1: Internally operating BF=0: Can accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address. Corresponds to cursor address. AC: Address counter used for both of DD and CG RAM address.	Execution time changes when frequency changes. (Example) When fcp or fosc is 270 KHz: $40\mu s \times \frac{250}{270} = 37\mu s$

* Dont' care

4.2 Description of Details

(1) Clear Display

	RS	R/W	DB7						DB0
Code	0	0	0	0	0	0	0	0	1

Writes space code "20"(hexadecimal) into all the DD RAM addresses.

The cursor returns to Address 0 (A_{DD}="00") and display, if it has been shifted, returns to the original position. In other words, display disappears and the cursor goes to the left edge of the display (the first line if 2 lines are displayed).

(2) Return Home

	RS	R/W	DB7						DB0	
Code	0	0	0	0	0	0	0	0	1	*

* (Don't Care)

Returns the cursor to Address 0 (A_{DD}="00") and display, if it has been shifted, to the original position. The DD RAM contents remain unchanged.

(3) Entry Mode Set

	RS	R/W	DB7						I/D	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

I/D: Increments (I/D=1) or decrements (I/D=0) the DD RAM address by one upon writing into or reading from the DD RAM a character code. The cursor moves to the right when incremented by one. The same applies to writing and reading of CG RAM.

S : Shifts the entire display to either the right or the left when S is 1; to the left when I/D=1 and to the right when I/D=0. Therefore, the cursor looks as if it stood still with the display only moved. Display is not shifted when reading from the DD RAM.

Display is not shifted when S=0.

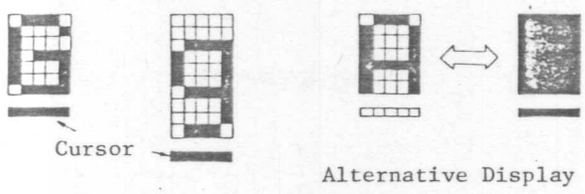
(4) Display ON/OFF Control

	RS	R/W	DB7						DB0	
Code	0	0	0	0	0	0	1	D	C	B

D : Display is turned ON when D=1 and OFF when D=0. When display is turned off due to D=0, the display data remains in the DD RAM and it can be displayed immediately by setting D=1.

C : The cursor is displayed when C=1 and not displayed when C=0. Even if the cursor disappears, function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7 dot character font is selected and in the 11th line when 5 × 10 dot character font is selected.

B : The character residing at the cursor position blinks when B=1. The blink is done by switching between all the black dots and display characters at 0.4 second interval. The cursor and the blink can be set concurrently.



5×7 Dot Character Font (a) Cursor Display Example

5×10 Dot Character Font (b) Blink Display Example

(5) Cursor or Display Shift

	RS	R/W	DB_7							DB_0	
Code	0	0	0	0	0	1	S/C	R/L	*	*	* (Don't Care)

Shifts the cursor position or display to the right and the left without writing or reading the display data. This function is used for correction or search of display.

S/C R/L

0 0 Shifts the cursor position to the left. (AC is decremented by one.)

0 1 Shifts the cursor position to the right. (AC is incremented by one.)

1 0 Shifts the entire display to the left. The cursor follows the display shift.

1 1 Shifts the entire display to the right. The cursor follows the display shift.

(6) Function Set

	RS	R/W	DB_7							DB_0	
Code	0	0	0	0	1	DL	N	F	*	*	* (Don't Care)

DL : Sets interface data length. Data is sent or received in 8 bit length ($DB_7 \sim DB_0$) when DL=1 and 4 bit length ($DB_7 \sim DB_4$) when DL=0. When 4 bit length is selected, data must be sent or received twice.

N : Sets number of display lines.

F : Sets character font.

N	F	No. of Display Lines	Character Font	Duty Factor	Remarks
0	0	1	5×7 dots	1/8	
0	1	1	5×10 dots	1/11	
1	*	2	5×7 dots	1/16	Cannot display 2 lines with 5×10 dot character font.

* (Don't Care)

(7) Set CG RAM Address

	RS	R/W	DB_7							DB_0
Code	0	0	0	1	A	A	A	A	A	A

←Higher Order Bits Lower Order Bits→

Sets the CG RAM address in a binary number of AAAAAA to the address counter, and data is written or read from the MPU related to the CG RAM after this.

(8) Set DD RAM Address

	RS	R/W	DB_7							DB_0
Code	0	0	1	A_N	A	A	A	A	A	A

← Higher Order Bits Lower Order Bits →

Sets the DD RAM address in a binary number of A_NAAAAAA to the address counter, and data is written or read from the MPU related to the DD RAM after this.

However, when N=0 (1-line display), A_NAAAAAA is "00"~"4F" (hexadecimal).

When N=1 (2-line display), A_NAAAAAA is "00"~"27" (hexadecimal) for the first line, and "40"~"67" (hexadecimal) for the second line.

(9) Read Busy Flag and Address

	RS	R/W	DB_7							DB_0
Code	0	1	BF	A	A	A	A	A	A	A

← Higher Order Bits Lower Order Bits →

Reads Busy Flag (BF) that indicates the system is internally operating on an instruction received before. When BF=1, it indicates that internal operation is going on and the next instruction is not accepted until BF is set to "0". Check the BF status before the next write operation.

At the same time, this value of the address counter expressed in a binary number of AAAAAA. The address counter is used by both of CG and DD RAM address, and its value is determined by the previous instruction.

Address contents are the same as Items (7) and (8).

(10) Write Data to CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	0	D	D	D	D	D	D	D	D

← Higher Order Bits Lower Order Bits →

Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM.

Whether the CG or the DD RAM is to be written is determined by the previous designation (CG RAM address setting or DD RAM address setting). After write, the address is automatically incremented or decremented by one according to entry mode. Display shift also follows the entry mode.

(11) Read Data from CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	1	D	D	D	D	D	D	D	D

← Higher Order Bits Lower Order Bits →

Reads binary 8 bit data DDDDDDDD from the CG or the DD RAM.

Whether the CG RAM or the DD RAM is to be read is determined by the previous designation. Prior to inputting this read instruction, either the CG RAM address set instruction or the DD RAM address set instruction must be executed. If it is not done, the first read data becomes invalid, and data of the next address is read normally from the second read.

After read, the address is automatically incremented or decremented by one according to the entry mode. However, display shift is not performed regardless of entry mode types.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power Supply Voltage (1)	VCC	-0.3 to +7.0	V	
Power Supply Voltage (2)	V1 to V5	VCC-13.5 to VCC+0.3	V	3
Input Voltage	VT	-0.3 to VCC+0.3	V	
Operating Tempertaure	Topr	-20 to +75	°C	
Storage Tempertaure	Tstg	-55 to +125	°C	

Note 1: When LSI's are used beyond the absolute maximum rating, LSI's may be permanently destroyed. Use under the electrical characteristic conditions is strongly recommended for normal operation. The use beyond these conditions, cause LSI's malfunction and at the same time undesirable effects on the reliability of the LSI's.

Note 2: All voltage values are referenced to GND=0V.

Note 3: Apply to V1 to V5. Must keep the relation of $V1 \geqq V2 \geqq V3 \geqq V4 \geqq V5$
(high ← → low)

5.2 Electrical Characteristics

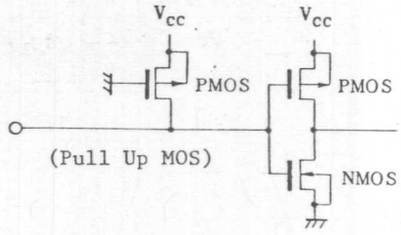
VCC=5V±10%
Ta=-20 to +75°C

Item	Symbol	Test Condition	Limit min	Limit typ	Limit max	Unit	Note
Input "High" Voltage	VIH		2.0	-	VCC	V	2
Input "Low" Voltage	VIL		-0.3	-	0.8	V	2
Output "High" Voltage(1)(TTL)	VOH1	-IOH=0.205mA	2.4	-	-	V	3
Output "Low" Voltage (1)(TTL)	VOL1	IOL=1.6mA	-	-	0.4	V	3
Output "High" Voltage(2)(CMOS)	VOH2	-IOH=0.04mA	0.9VCC	-	-	V	4
Output "Low" Voltage(2)(CMOS)	VOL2	-IOH=0.04mA	-	-	0.1VCC	V	4
Driver Voltage Descending(COM)	Vd1	Id=0.1mA	-	-	1.0	V	
Driver Voltage Descending(SEG)	Vd2	Id=0.01mA	-	-	0.2	V	
Input Leakage Current	IIL	Vin=0 to VCC	-	-	1	µA	5
Pull up MOS Current	-IP	VCC=5V	2	10	20	µA	
Power Supply Current	ICC1	Ceramic Filter Oscillation	-	0.4	1.0	mA	6
Power Supply Current (2)	ICC2	Rf Oscillation, External Clock Operation	-	0.2	0.5	mA	6
External Clock Operation							
External Clock Frequency	fcp		125	250	300	kHz	7
External Clock Duty	Duty		45	50	55	%	7
External Clock Rise Time	Trcp		-	-	0.2	µs	7
External Clock Fall Time	Tfcp		-	-	0.2	µs	7
Internal Clock Operation(Rf Oscillation)							
Clock Oscillation Frequency	fosc	Rf=91kΩ±2%	190	250	310	kHz	8
Internal Clock Operation(Ceramic Filter Oscillation)							
Clock Oscillation Frequency	fosc	Ceramic Filter	245	250	255	kHz	9

Note 1: The following shows the configurations of I/O terminals except liquid crystal display output.

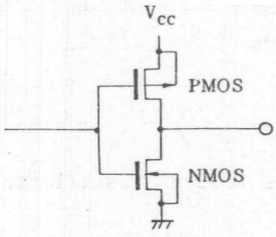
·Figure of Input Terminal

Applicable Terminals : RS, R/W, E



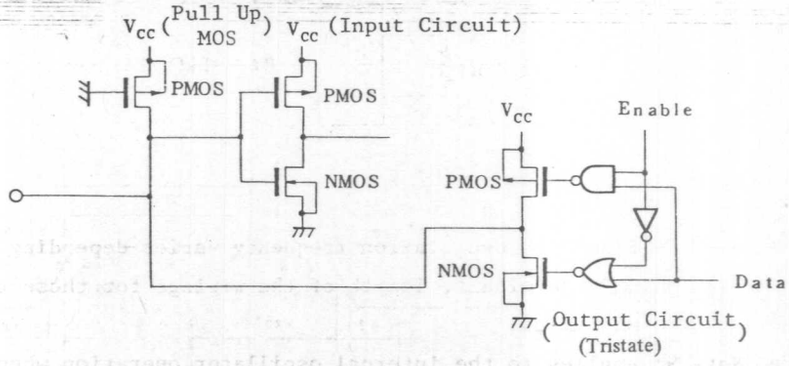
·Figure of Output Terminal

Applicable Terminals : CL_1, CL_2, M, D



·Figure of I/O Terminal

Applicable Terminals : $DB_0 \sim DB_7$



Note 2: Applies to the input terminals and the I/O terminals.

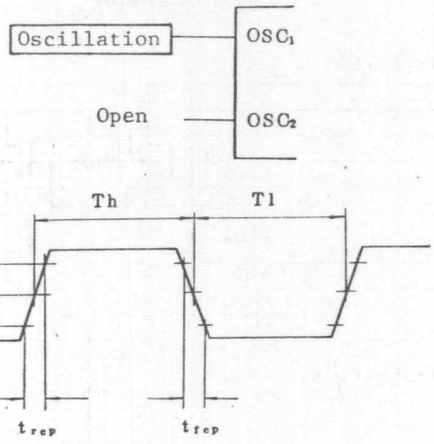
Note 3: Applies to the I/O terminals.

Note 4: Applies to the output terminals.

Note 5: Current that flows through pull-up MOS's and output drive MOS's is excluded.

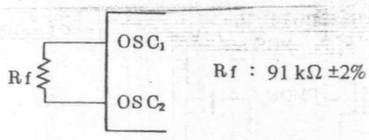
Note 6: Current that flows through pull-up MOS'a is excluded. With CMOS, when input is in the intermediate level, excessive current flows through the input circuit to the power supply. In order to avoid this, input level must be settled high or low.

Note 7: Applies to the external clock operation.



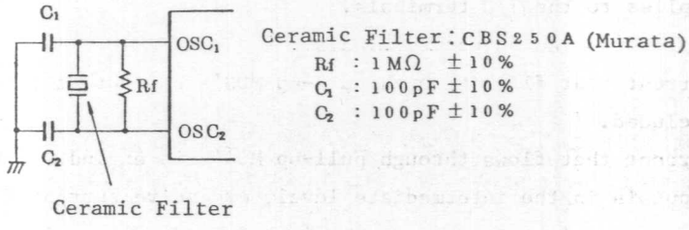
$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

Note 8: Applies to the internal oscillator operation when oscillation resistor Rf is used.



Since the oscillation frequency varies depending on capacity of OSC_1 and OSC_2 terminals, length of the wirings for these terminals should be minimized.

Note 9: Applies to the internal oscillator operation when a ceramic filter is used.



5.3 Timing Characteristics (V_{CC} = 5V ±10%, Ta = -20 to +75°C)

Item	Symbol	Test Conditions	Limit			Unit
			min	typ	max	
Enable Cycle Time	t_{cyc}	Fig.5.1, Fig.5.2	3.0	-	-	μs
Enable Pulse Width	PW_{EH}	Fig.5.1, Fig.5.2	1.8	-	-	μs
Enable Rise/Fall Time	t_{Er}, t_{Ef}	Fig.5.1, Fig.5.2	-	-	2.0	μs
Address Set-up Time	t_{AS}	Fig.5.1, Fig.5.2	0.9	-	-	μs
Data Delay Time	t_{DDR}	Fig.5.2	-	-	0.9	μs
Data Set-up Time	t_{DSW}	Fig.5.1	0.9	-	-	μs
Hold Time	t_H	Fig.5.1, Fig.5.2	0.9	-	-	μs
Clock Pulse Width("High"Level)	t_{CWH}	Fig.5.3	1.5	-	-	μs
Clock Pulse Width("Low"Level)	t_{CWL}	Fig.5.3	1.5	-	-	μs
Clock Set-up Time	t_{CSU}	Fig.5.3	1.5	-	-	μs
Data Set-up Time	t_{SU}	Fig.5.3	1.5	-	-	μs
Data Hold Time	t_{DH}	Fig.5.3	1.5	-	-	μs
M Delay Time	t_{DM}	Fig.5.3	-1.5	-	1.5	μs

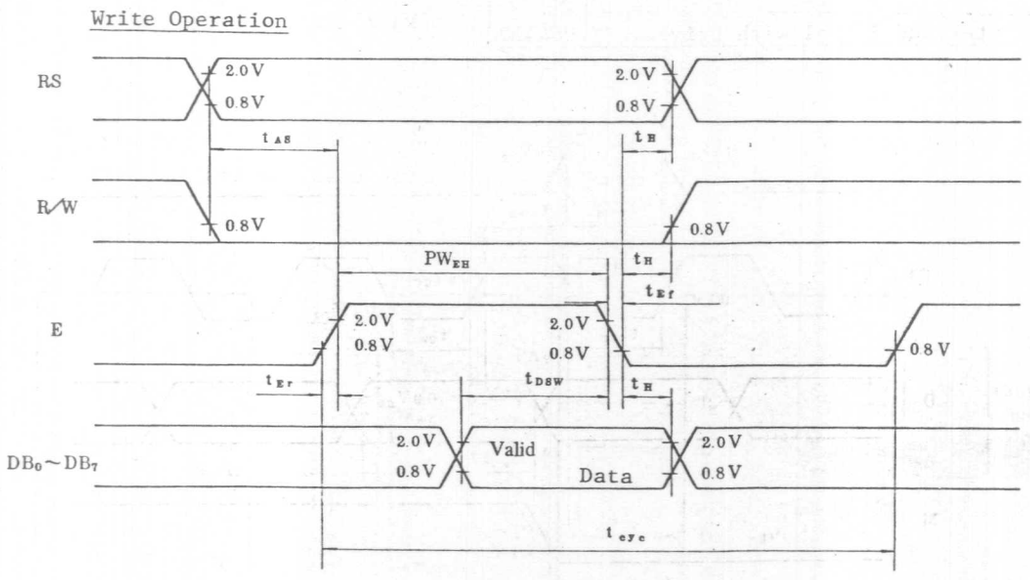


Fig. 5.1 Writing Data from MPU to HD44780

Read Operation

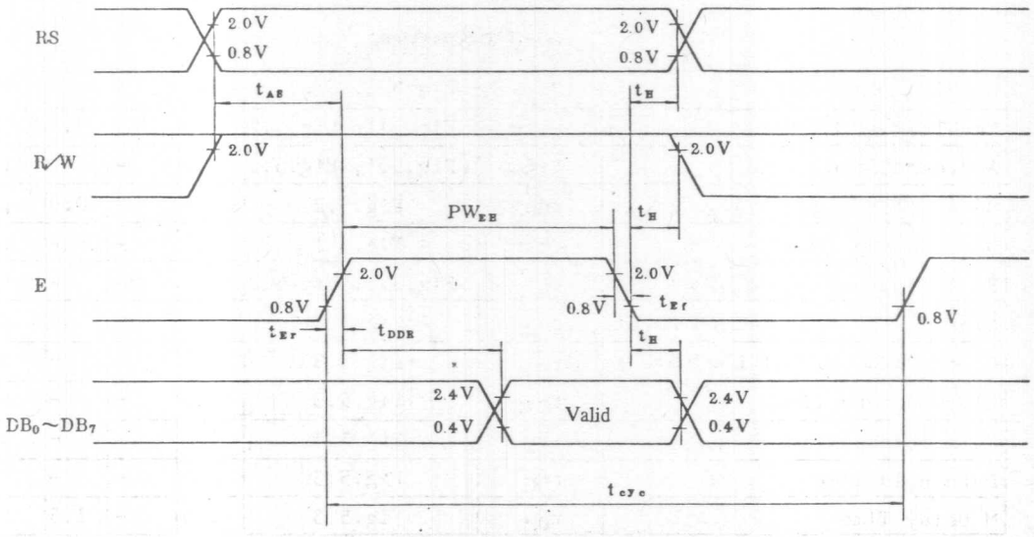


Fig. 5.2 Reading Data from HD44780 to MPU

Interface Signal with Driver LSI HD44100

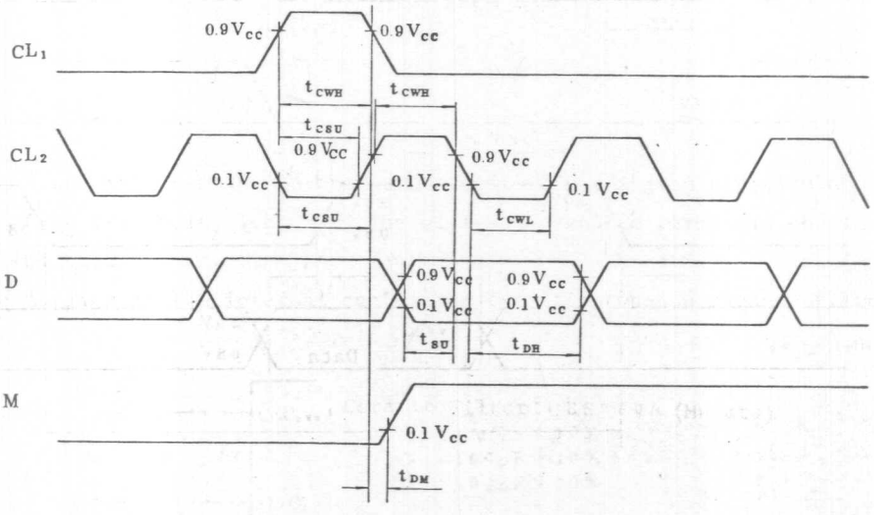


Fig. 5.3 Sending Data to Driver LSI HD44100

6. How to Use HD44780

6.1 Interface to MPU

(1) Interface to 8-bit MPU

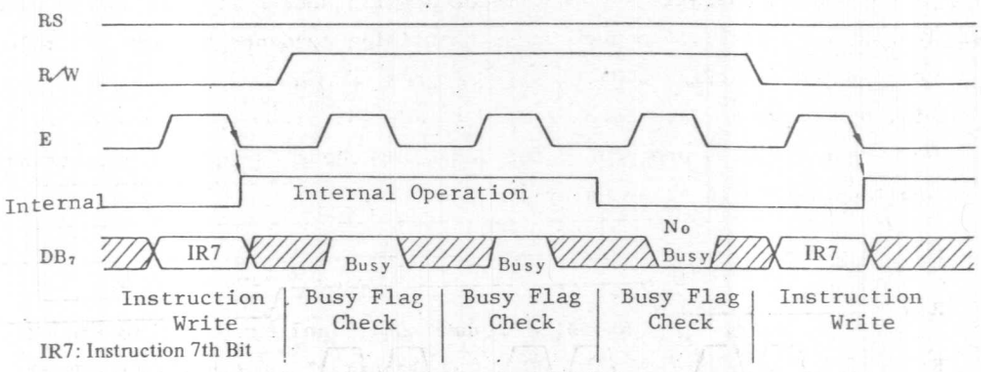


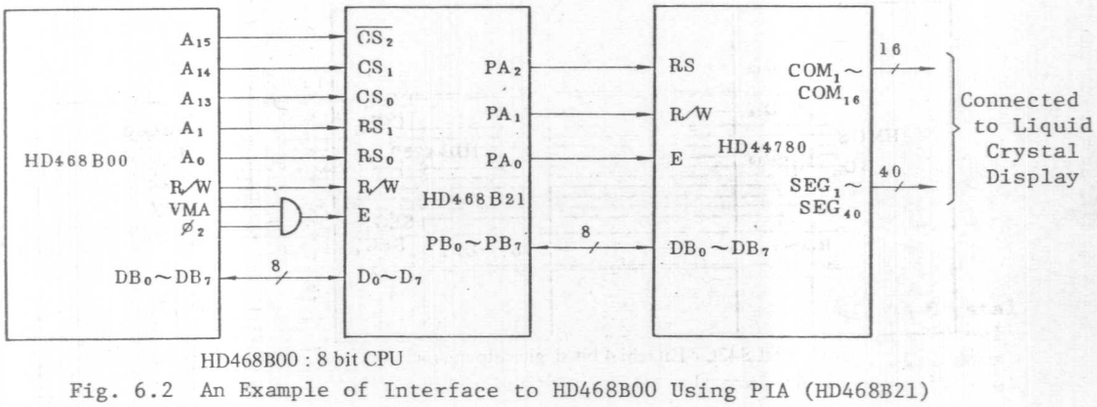
Fig. 6.1 An Example of Busy Flag Check Timing Sequence

Since the HD44780 cannot be directly connected to MPU address bus and data bus PIA or I/O port (in the case of single chip microcomputer) is needed as an interface device. Input and output of the interface device is TTL compatible.

Fig. 6.2 shows a circuit example.

In the example, $PB_0 \sim PB_7$ are connected to the data bus $DB_0 \sim DB_7$ and $PA_0 \sim PA_2$ are connected to E, R/W and RS respectively.

Attention must be paid to the timing relation between E and other signals when reading ot writing data using PIA as an interface.



HD468B00 : 8 bit CPU

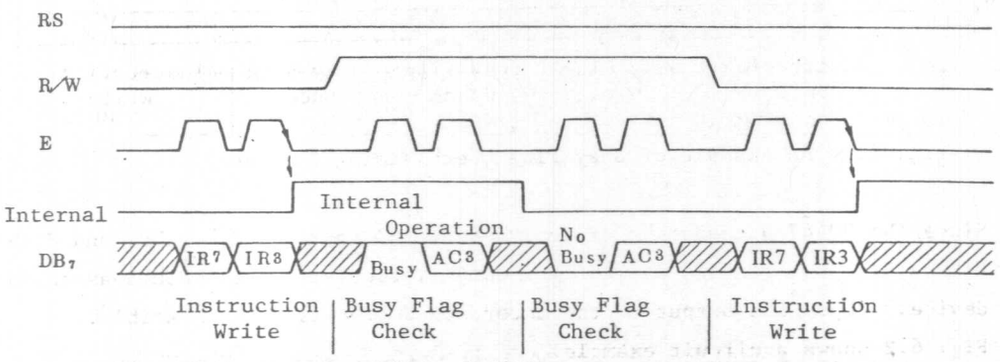
Fig. 6.2 An Example of Interface to HD468B00 Using PIA (HD468B21)

(2) Interface to 4-bit MPU

The HD44780 can be connected to 4-bit MPU through 4-bit MPU I/O port. If the I/O port has enough bits, data can be transfered in 8-bit length, but if not in two operations of 4 bits each (with designation of interface data length for 4 bits). In such case, the timing sequence becomes a little complicated (See Fig. 6.3).

Fig. 6.4 shows an interface example to HMCS43C.

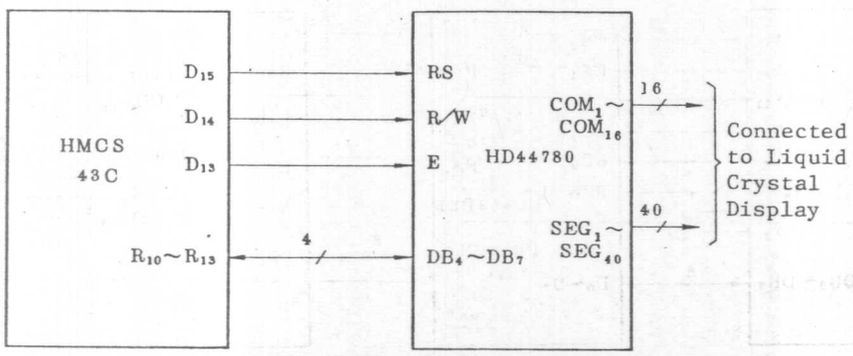
Note that 2 cycles are needed for busy flag check as well as data transfer. 4-bit operation is selected by program.



Note : IR7, IR3: Instruction 7th bit , 3rd bit

AC3 : Addres Counter 3rd bit

Fig. 6.3 An Example of 4-bit Data Transfer Timing Sequence



HMCS43C : Hitachi 4 bit single chip microcomputer

Fig. 6.4 An Example of Interface to HMCS43C

6.2 Interface to Liquid Crystal Display

(1) Character Font and Number of Lines

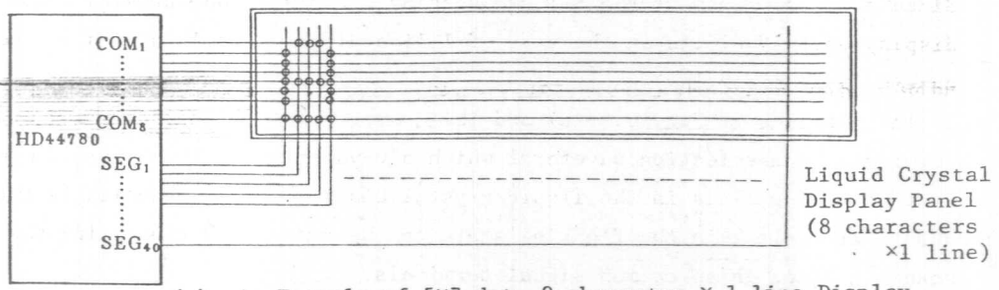
The HD44780 can perform 2 types of display, 5×7 dots and 5×10 dots as character font, with a cursor on each of them. Number of display lines is up to 2 lines with 5×7 dots and 1 line with 5×10 dots. Therefore, number of common signals available are the following three types:

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5×7 dots + Cursor	8	1/8
1	5×10 dots + Cursor	11	1/11
2	5×7 dots + Cursor	16	1/16

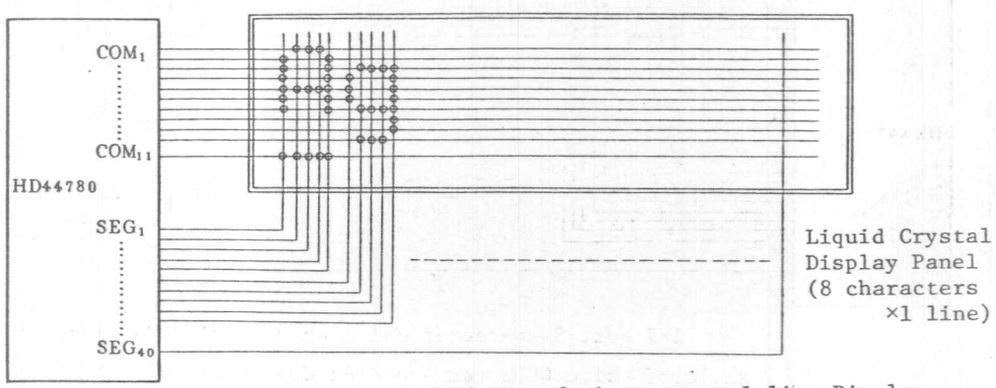
Number of lines and font types can be selected by program.
(refer to Chapter 4, Instruction)

(2) Connection to HD44780 and Liquid Crystal Display

Fig. 6.5 (1) and (2) show connection examples.

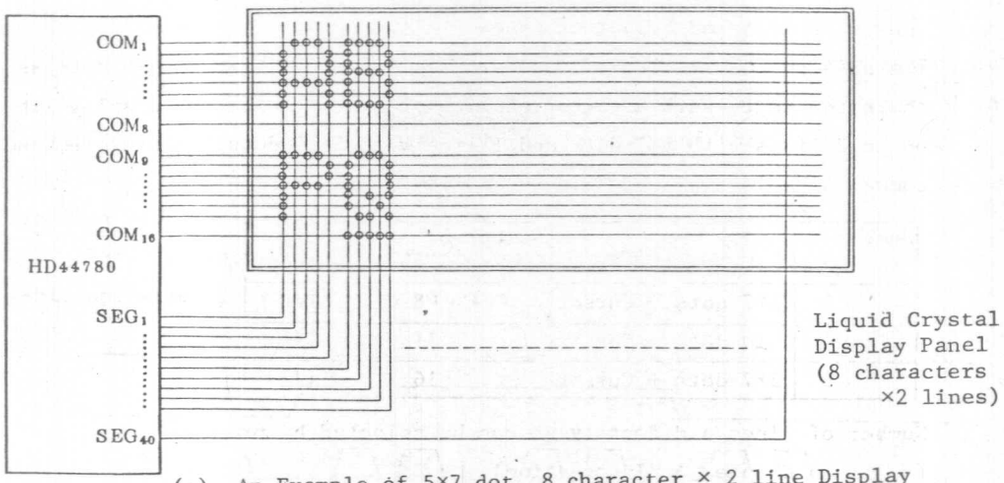


(a) An Example of 5×7 dot, 8 character × 1 line Display
(1/4 Bias, 1/8 Duty)



(b) An Example of 5×10 dot, 8 character × 1 line Display
(1/4 Bias, 1/11 Duty)

Fig. 6.5 (1) Examples of Connection to HD44780 and Liquid Crystal Display

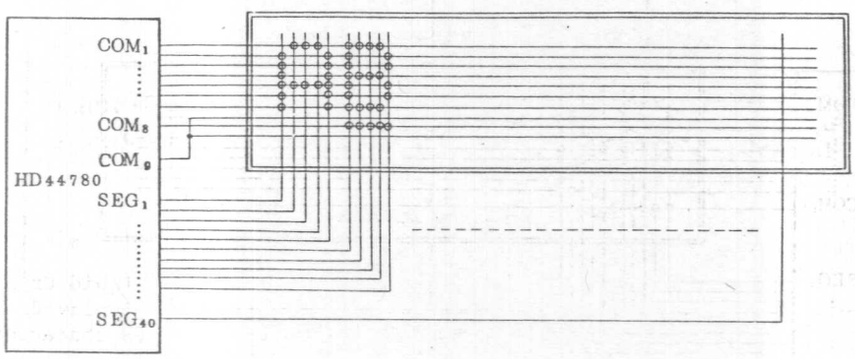


(c) An Example of 5×7 dot, 8 character × 2 line Display (1/5 Bias, 1/16 Duty)

Fig. 6.5 (2) An example of Connection to HD44780 and Liquid Crystal Display

Since 5 signal lines at the SEG can display one digit, one HD44780 can display up to 8 digits in the case of 1-line display and 16 digits in the case of 2-line display.

In the examples of Fig. 6.5 (a) and (b), there are some unused common signal terminals, non-selection waveforms which always output. When there are unused extra scanning lines in the liquid crystal display panel, undesirable influence due to cross-talk in the floating state can be avoided by connecting the extra scanning lines these common signal terminals.



5×7 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)

Fig. 6.6 An Example of Using COM_9 for Avoiding Cross-talk of the Unneeded Scanning Line

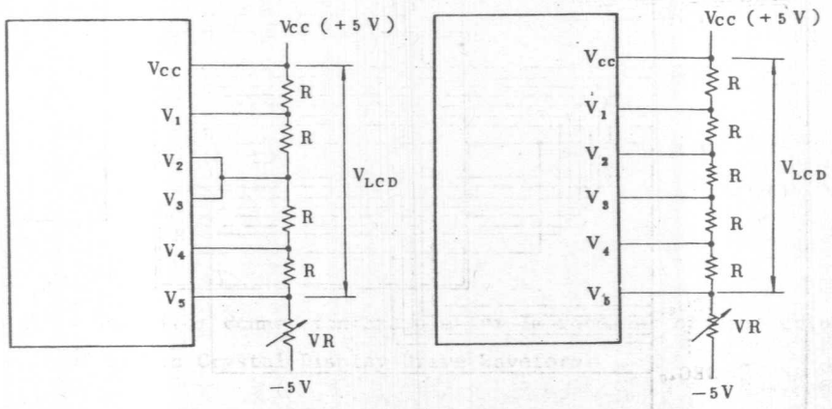
6.3 Power Supply for Liquid Crystal Display Drive

Various levels of voltage must be applied to the HD44780 terminals V_1 to V_5 in order to obtain drive waveforms of liquid crystal display. These voltages must be changed according to duty factors. Table 6.1 shows the relation.

Table 6.1 Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty Factor / Bias / Power Supply	1/8, 1/11 1/4	1/16 1/5
V_1	$V_{cc} - 1/4\ V_{LCD}$	$V_{cc} - 1/5\ V_{LCD}$
V_2	$V_{cc} - 1/2\ V_{LCD}$	$V_{cc} - 3/5\ V_{LCD}$
V_3	$V_{cc} - 1/2\ V_{LCD}$	$V_{cc} - 3/5\ V_{LCD}$
V_4	$V_{cc} - 3/4\ V_{LCD}$	$V_{cc} - 4/5\ V_{LCD}$
V_5	$V_{cc} - V_{LCD}$	$V_{cc} - V_{LCD}$

V_{LCD} gives peak values of liquid crystal display drive waveforms.
Each voltages can be given by resistance dividing as shown in Fig. 6.8.



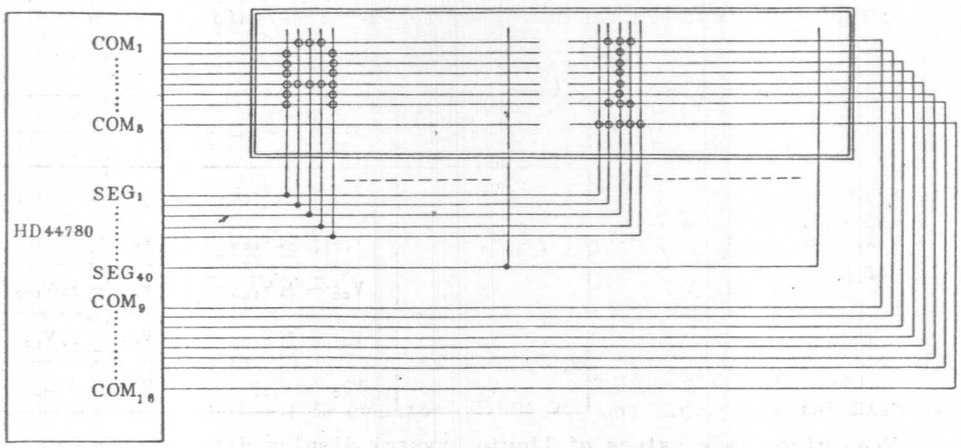
(a) 1/4 Bias (1/8, 1/11 Duty)

(b) 1/5 Bias (1/16 Duty)

Fig. 6.8 Drive Voltage Supply Example

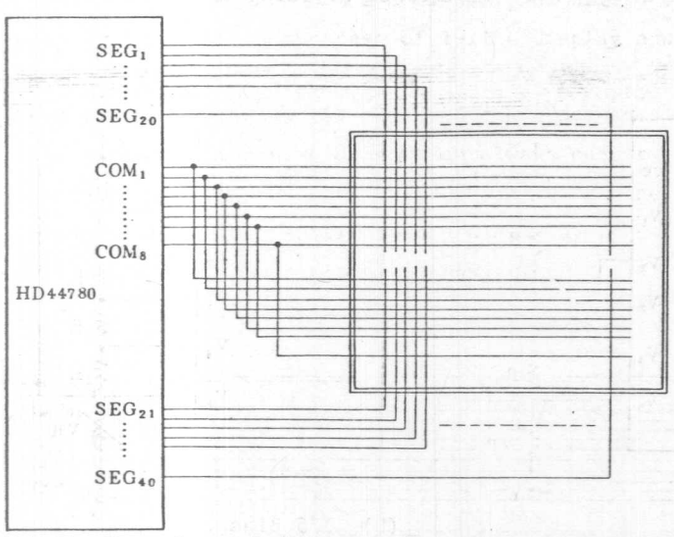
(3) Connection of Changed Matrix Layout

In the preceding examples, number of lines were corresponded to scanning lines. The following types of displays are possible by changing layout of the matrix configuration in the liquid crystal display panel.



(a) An Example of 5×7 dot, 16 character × 1 line Display

(1/5 Bias, 1/16 Duty)



(b) An Example of 5×7 dot, 4 character × 2 line Display

(1/4 Bias, 1/8 Duty)

Fig. 6.7 A Display Example of Changed Matrix Layout

In either case, the change is only on the layout and display characteristics and number of display characters of liquid crystal are dependent on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) addresses for 8 characters × 2 lines and 16 characters × 1 line are the same as shown in Fig. 6.5.

Resistance value is determined in consideration of operation margin and power consumption. Since liquid crystal display load is capacitive, drive waveform itself is distorted by charge/discharge current when the liquid crystal display drive waveform is applied. To minimize the distortion, the resistance value must be made smaller, but this increases the current flown through the dividing resistors causing higher power consumption.

Since larger liquid crystal display panels have larger capacitance, resistance value must be made smaller.

Adding capacitors in parallel to resistors, as shown in Fig. 6.9, is effective to improve charge/discharge distortions. However, there is a limit in the effect. Level shift occurs and operation margin cannot be improved even if attempts are made in reducing power consumption with large resistance and in improving waveform distortion with large capacitance.

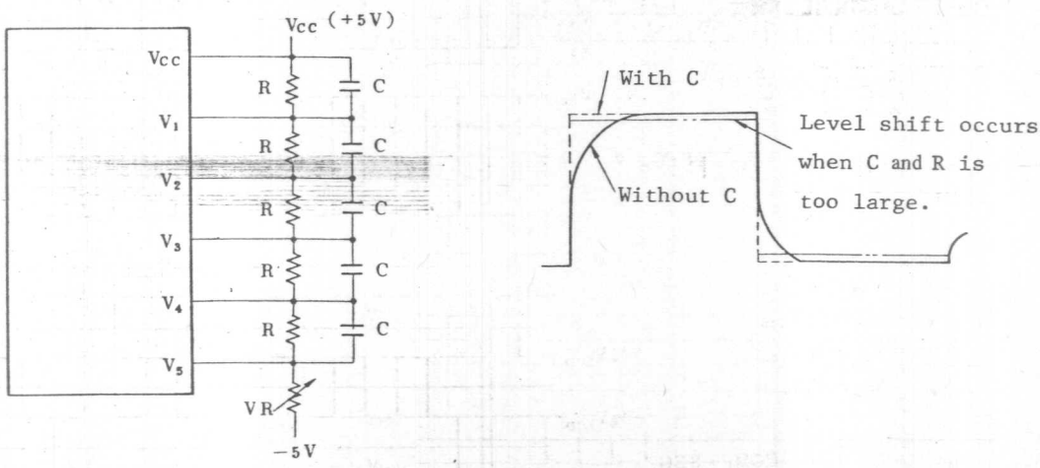


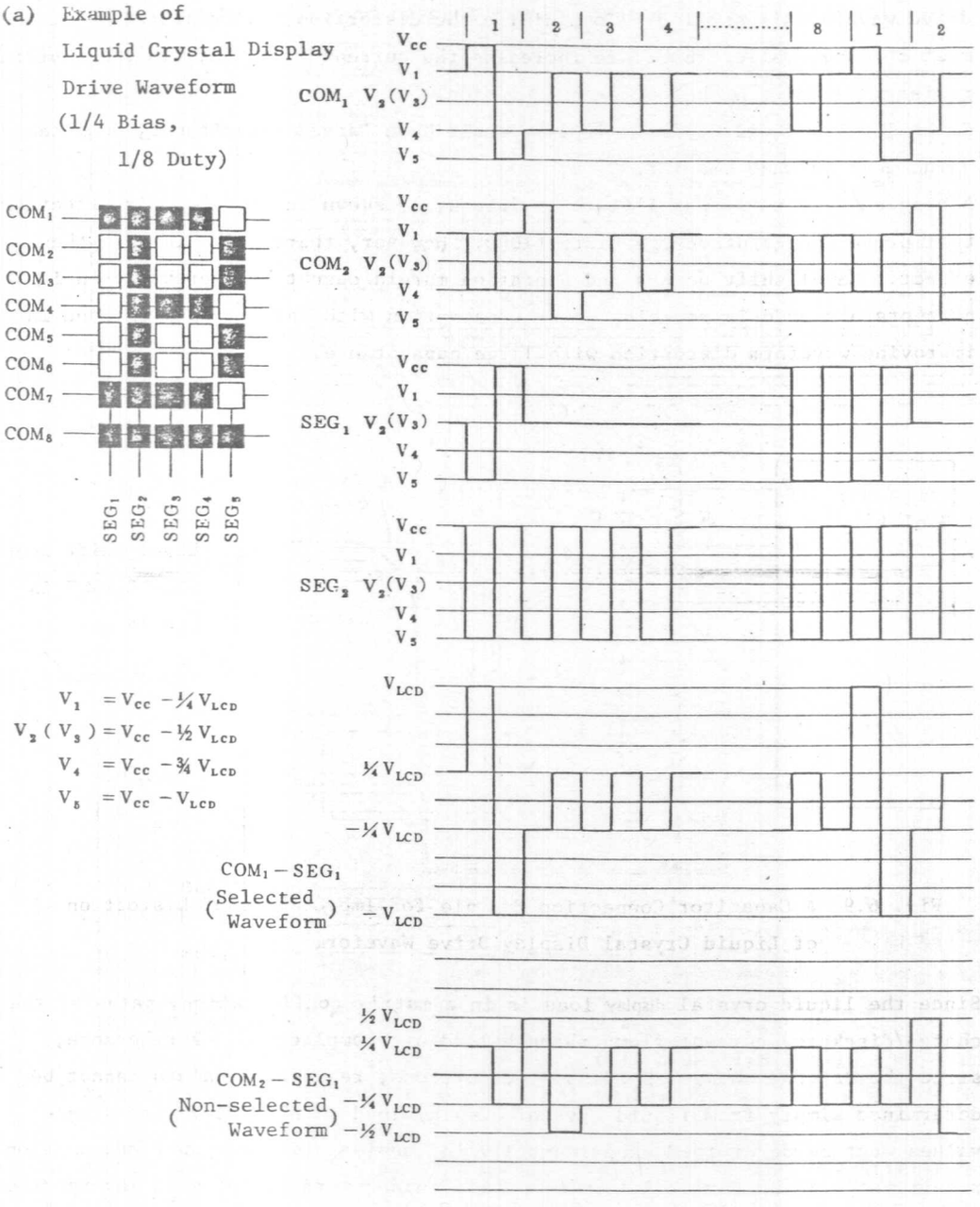
Fig. 6.9 A Capacitor Connection Example for Improvement of Distortion of Liquid Crystal Display Drive Waveform

Since the liquid crystal display load is in a matrix configuration, paths of the charge/discharge current flown through load are complicated. Furthermore, since the current changes by display conditions, resistance values cannot be determined simply from liquid crystal display load capacitance. Resistance values must be determined experimentally in consideration of power consumption requiremant of the device into which the liquid crystal display is incorporated. Generally, R=1～10kΩ and VR=5～50kΩ are used without using capacitors. Capacitors, if they are used, are usually of 0.1μF or less.

6.4 Liquid Crystal Display Drive Waveform

Examples of voltage levels and liquid crystal display drive waveforms are shown below.

(a) Example of Liquid Crystal Display Drive Waveform (1/4 Bias, 1/8 Duty)



$V_1 = V_{CC} - 1/4\ V_{LCD}$

$V_2 (V_3) = V_{CC} - 1/2\ V_{LCD}$

$V_4 = V_{CC} - 3/4\ V_{LCD}$

$V_5 = V_{CC} - V_{LCD}$

Fig. 6.10 Example of Liquid Crystal Display Drive Waveform (1)

(b) Example of Liquid Crystal Display Drive Waveform (1/5 Bias, 1/16 Duty)

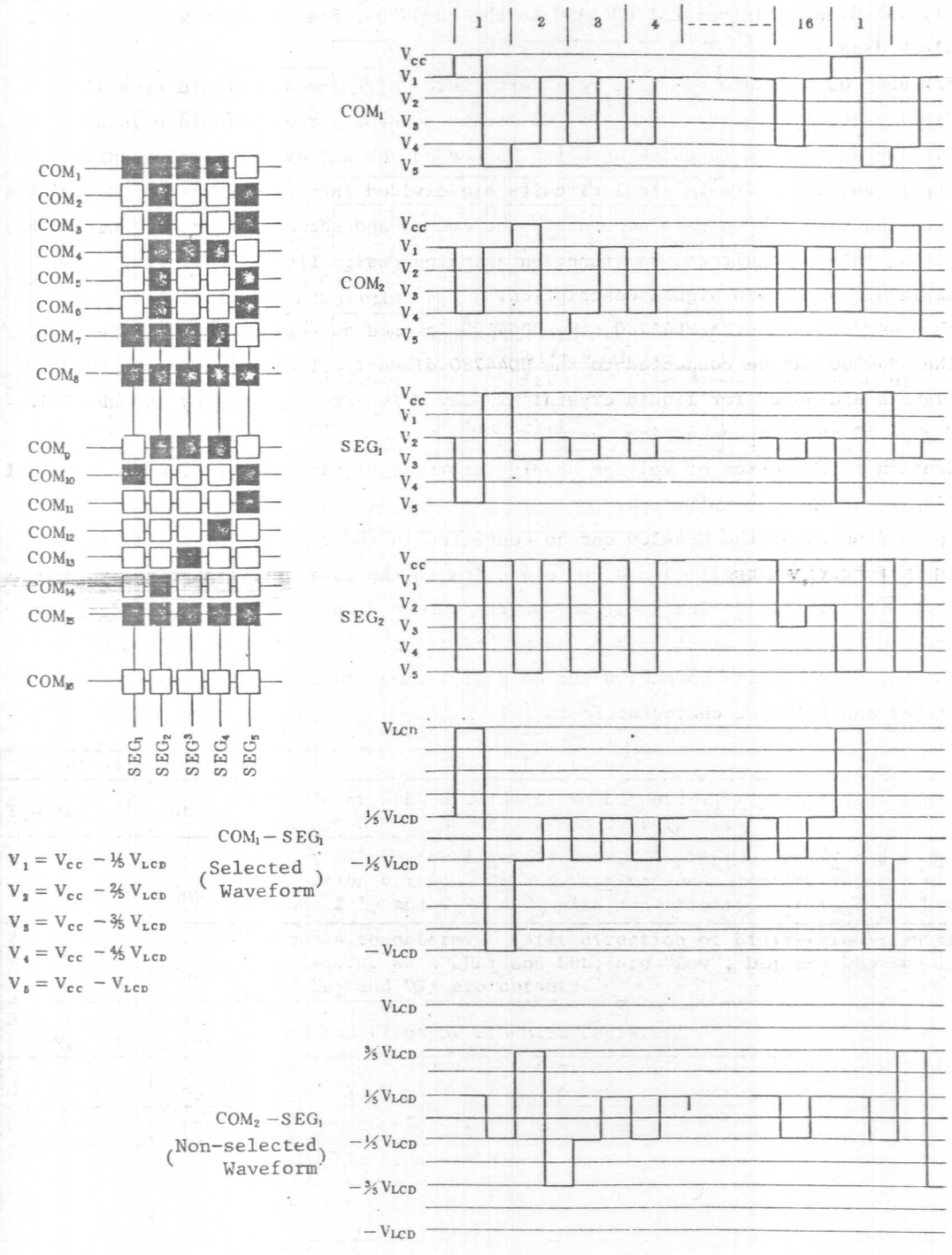


Fig. 6.10 Example of Liquid Crystal Display Drive Waveform (2)

6.5 Connection with Driver LSI HD44100

Number of display digits can be increased by externally connecting a liquid crystal display driver LSI HD44100 to the HD44780. Fig. 6.11 shows the HD44100 block diagram.

The HD44100 consists of shift registers, latch circuits and liquid crystal display drive circuits. The HD44100 is the general purpose liquid crystal display driver LSI to which any bias balues can be set by externally applying supply voltage. Its internal circuits are divided into 2 channels of 20 circuits each and they can be used separately for common and segment signals. The shift registers have bidirectional function allowing design flexibility.

Table 6.2 shows I/O signal description.

When connected to the HD44780, the HD44100 is used as segment signal driver. The HD44100 can be connected to the HD44780 directly since CL_1, CL_2, M and D signals and power for liquid crystal display drive are supplied by the HD44780. Fig. 6.12 shows a connection example.

Caution : Connection of voltage supply terminals V_1 through V_2 for liquid crystal display drive is complicated.

Up to 9 units of the HD44100 can be connected in the case of 1-line display (duty factor 1/8 or 1/11) and up to 4 units in the case of 2-line display (duty factor 1/16). The limit is due to maximum display digit numbers for the HD44780 being 80 characters because of RAM size. The connection method shown in Fig. 6.12 remains unchanged for both of 1-line and 2-line display or for both of 5×7 and 5×10 dot character fonts.

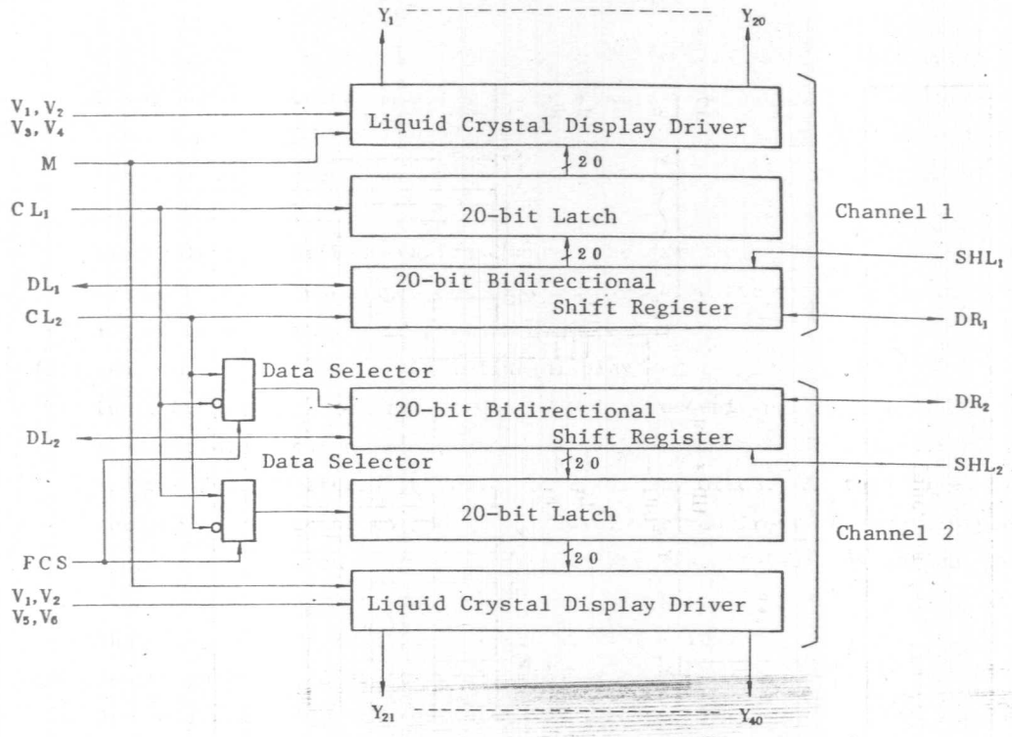


Fig. 6.11 HD44100 Block Diagram

Table 6.2 HD44100 Terminal Function Description

Signal Name	I/O	Function
$Y_1 \sim Y_{40}$	Output	Liquid crystal display drive output. Y_1 Y_{20} and Y_{21} Y_{40} correspond to Channels 1 and 2, respectively.
$V_1 \sim V_6$	Input	Power supply for liquid crystal display drive. V_1 and V_2 give selection voltage, V_3 and V_4 give non-selection voltage of Channel 1, and V_5 and V_6 give non-selection voltage of Channel 2.
SHL_1, SHL_2	Input	Signals to determine shift direction of bidirectional shift registers. When SHL_1 and SHL_2 are "Low", DL_1 and DL_2 are inputs and DR_1 and DR_2 are outputs.
DL_1, DL_2, DR_1, DR_2	Input/ Output	Data input/output of shift registers
M	Input	Signal to convert liquid crystal display drive output to AC. V_1/V_2, V_3/V_4 and V_5/V_6 are output alternatively.
CL_1, CL_2	Input	Data shift clock (CL_2) and latch clock (CL_1)
FCS	Input	Mode selection signal for Channel 2. It can be used for segment signal drive when FCS is "Low" and for common signal drive when FCS is "High". Channel 1 remains unchanged (It is for segment signal).

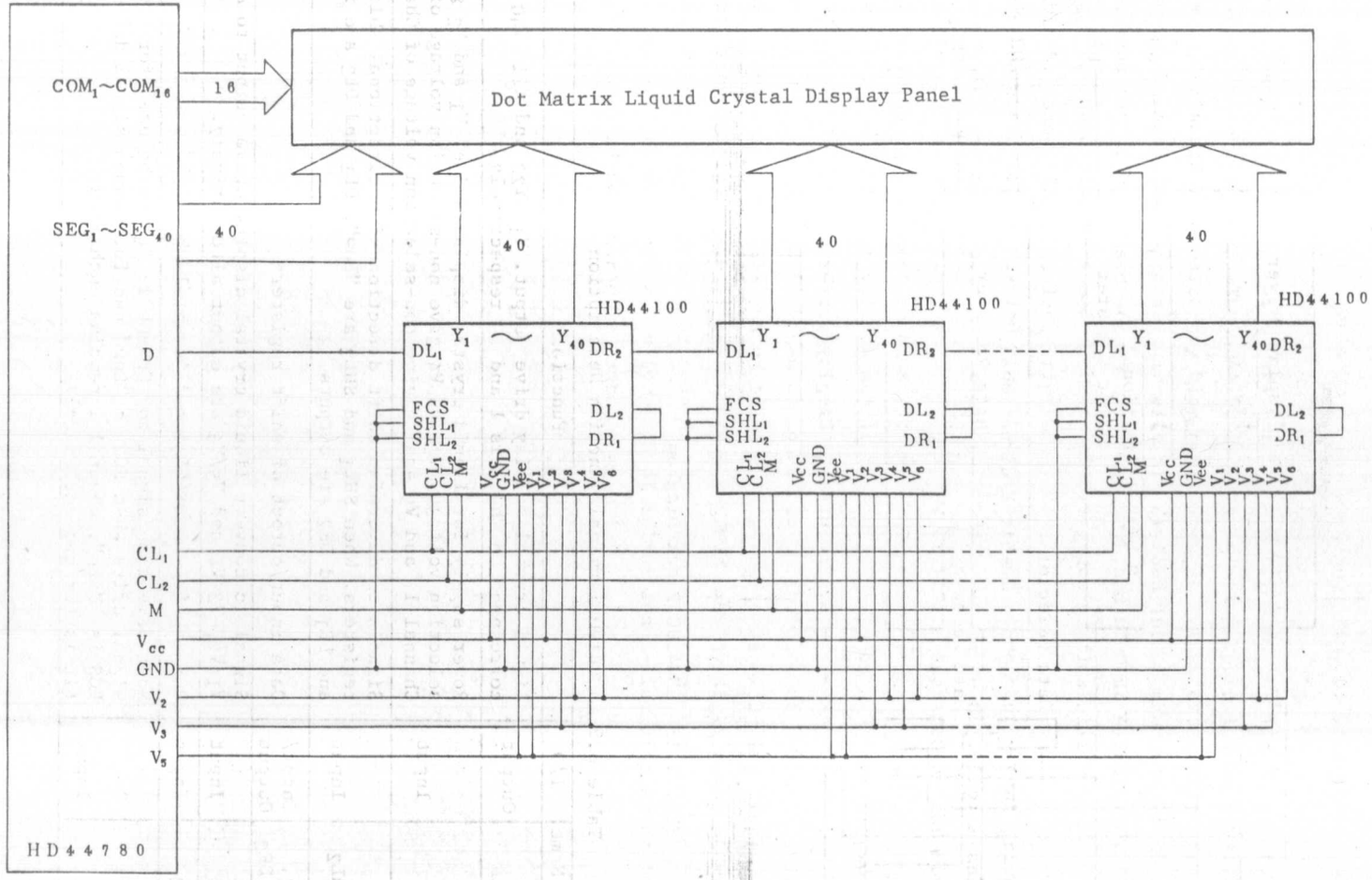


Fig.6.12 Connection HD44100S to HD44780

6.6 Correspondence Example of Instructions and Display

(1) 8-bit Operation, 8-digit × 1-line Display

Table 6.3 shows a display example of 8-digit × 1-line in 8-bit operation. The HD44780 functions must be set by Function Set prior to display.

Since display data RAM can store data for 80 chatacters, as explained before, the RAM can be used to display like lightning board when combined with display shift operation.

Since display shift operation changes the display position only and the DD RAM contents remain unchanged, display data entered first can be output when return home operation is performed.

(2) 4-bit operation, 8-digit × 1-line display

Function set by a program is needed prior to 4-bit operation. Table 6.4 shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as 8-bit operation. At this time, since nothing is connected to $DB_0 \sim DB_3$, rewrite is required. However, since one operation completes in two accesses in the case of 4-bit operation, rewrite is needed as function (see Table 6.4)

Thus, $DB_4 \sim DB_7$ of function set are written twice.

(3) 8-bit Operation, 8 digit × 2-line display

For 2-line display, the cursor moves from the first line to the second line automatically after write into the 40th digit of the 1st line is finished. Therefore, if there are only 8 digits in the first line, the DD RAM address must be set again after completion of the 8th digit. (see Table 6.5)

Note that the first and second lines of the display shift are performed. In the example, display shift is performed when the cursor is on the second line. However, if shift operation is performed when the cursor is on the first line, both the first and the second lines move concurrently. When shift is repeated, display of the second line does not move to the first line, but the same display only moves in each line many times.

Table 6.3 8-bit Operation, 8-digit × 1-line Display

Instruction	Display	Operation
Power Supply ON (Internal Reset Circuit)		Initialized. No display appears.
Function Set RS R/W DB7 ~ DB0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display and 5×7 dot character font.
Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. All display is in space mode because of initialization.
Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
Write Data to CG RAM/ DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by the initialization performed when the power is turned on. The cursor is incremented by one and shifted to the right.
Write Data to CG/RAM DD RAM 1 0 0 1 0 0 1 0 0 1	HI_	Writes "I".
⋮	⋮	
Write Data to CG/RAM DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI_	Sets mode for display shift at the time of write.
Write Data to CG RAM/ DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI _	Writes "space".
Write Data to CG RAM/ DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M_	Writes "M".
⋮	⋮	
Write Data to CG RAM/ DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO_	Writes "O".
Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
Write Data to CG RAM/ DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO_	Shifts only the cursor position to the right.
Write Data to CG RAM/ DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM_	Writes "M".
Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both of the display and cursor to the original position (Address 0).

Table 6.4 4-bit Operation, 8-digit 1-line Display Example

Instruction	Display	Operation
Power Supply ON (Internal Reset Circuit)		Initialized. No display appears.
Function Set RS R/W DB7 ~ DB4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets 4-bit operation and selects 1-line display and 5×7 dot character font. 4-bit operation starts from this point on and resetting is needed.
Display ON/OFF Control 0 0 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. All display is in space mode because of initialization.
Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
Write Data to CG RAM/ DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H _	Writes "H". The cursor is incremented by one and shifts to the right.

Hereafter, control is the same as 8-bit operation.

Table 6.5 8-bit Operation, 8-digit × 2-line Display Example

Instruction	Display	Operation
Power Supply ON (Internal Reset Circuit)		Initialized. No display appears.
Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and 5×7 dot character font.
Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. All display is in space mode because of initialization.
Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
Write Data to CG RAM/ DD RAM 1 0 0 1 0 0 1 0 0 0	H _	Writes "H". The DD RAM has already been selected by the initialization performed when the power is turned on. The cursor is incremented by one and shifted to the right.
⋮	⋮	
Write Data to CG RAM/ DD RAM 1 0 0 1 0 0 1 0 0 1	H I T A C H I _	Writes "I".
Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	H I T A C H I _	Sets RAM address so that the cursor is positioned at the head of 2nd line.
Write Data to CG RAM/ DD RAM 1 0 0 1 0 0 1 1 0 1	H I T A C H I M _	Writes "M".
⋮	⋮	
Write Data to CG RAM/ DD RAM 1 0 0 1 0 0 1 1 1 1	H I T A C H I M I C R O C O _	Writes "O".
Entry Mode Set 0 0 0 0 0 0 0 1 1 1	H I T A C H I M I C R O C O _	Sets mode for display shift at the time of write.
Write Data to CG RAM/ DD RAM 1 0 0 1 0 0 1 1 0 1	I T A C H I I C R O C O M _	Writes "M". Display is shifted to the right. The First line's and the second line's shift are operated at the same time.
⋮	⋮	
Return Home 0 0 0 0 0 0 0 0 1 0	H I T A C H I M I C R O C O M	Returns both of the display and cursor to the original position (Address 0).

7. Appendix

Specification of HD44100

(1) Absolute Maximum Ratings

Item	Symbol	Limit	Unit
Power Supply Voltage (1)	VCC	-0.3 to +7.0	V
Power Supply Voltage (2)	Vee, V1 to V6	VCC-13.5 to VCC+0.3	V
Input Voltage	VT	-0.3 to VCC+0.3	V
Operating Tempertaure	Topr	-20 to +75	°C
Storage Tempertaure	Tstg	-55 to +125	°C

Note 1: When LSI's are used beyond the absolute maximum rating, LSI's may be permanently destroyed. Use under the electrical characteristic conditions is strongly recommended for normal operation. The use beyond these conditions, cause LSI's malfunction and at the same time undesirable effects on the reliability of the LSI's.

Note 2: All voltage values are referenced to GND=0V.

(2) Electrical Characteristics
(VCC=5V+10%, Vee, V1 to V6=-4 to -6 , Ta=-10 to +70°C)

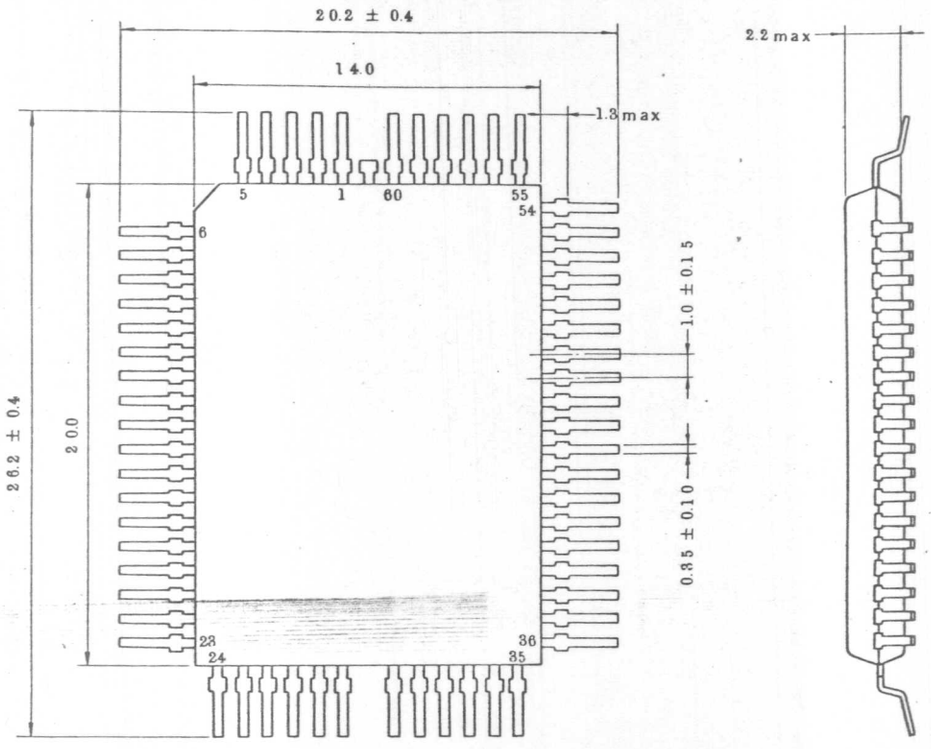
Item	Symbol	min	typ	max	Unit	Note
Input "High" Voltage	VIH	0.7VCC	-	-	V	(1)
Input "Low" Voltage	VIL	-	-	0.3VCC	V	(1)
Output "High" Voltage(-IOH=0.4mA)	VOH	VCC-0.4	-	-	V	(2)
Output "Low" Voltage(IOL=0.4mA)	VOL	-	-	0.4	V	(2)
Y1 to Y40 Driver Voltage Descending	Vd1	-	-	1.1	V	
	Vd2	-	-	1.5	V	
Input Leakage Frequency	+IIL	-	-	5.0	A	
Power Supply Current Logic Part(fCL2=400kHz)	ICC	-	-	1.0	mA	
Liquid Crystal Display Drive Part (fM=1kHz)	-Iee	-	-	10.0	µA	

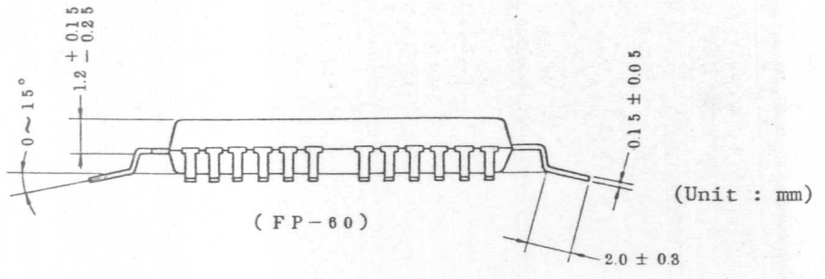
Note: Applicable Terminal
(1) CL1, CL2, DL1, DL2, DR1, DR2, M, SHL1, SHL2, FCS
(2) DL1, DL2, DR1, DR2

(3) Table of HD44100 Pin Assignment

Pin No	Power Supply	Input	Output		Pin No	Power Supply	Input	Output
1			Y_{30}		31			Y_5
2			Y_{31}		32			Y_4
3			Y_{32}		33			Y_3
4			Y_{33}		34			Y_2
5			Y_{34}		35			Y_1
6			Y_{29}		36	Vee		
7			Y_{28}		37		CL_1	
8			Y_{27}		38		CL_2	
9			Y_{26}		39	GND		
10			Y_{25}		40		DL_1	DL_1
11			Y_{24}		41		DR_1	DR_1
12			Y_{23}		42		DL_2	DL_2
13			Y_{22}		43		DR_2	DR_2
14			Y_{21}		44	NC		
15			Y_{20}		45		M	
16			Y_{19}		46		SHL_1	
17			Y_{18}		47		SHL_2	
18			Y_{17}		48		FCS	
19			Y_{16}		49	V_1		
20			Y_{15}		50	V_2		
21			Y_{14}		51	V_3		
22			Y_{13}		52	V_4		
23			Y_{12}		53	V_5		
24			Y_9		54	V_6		
25			Y_{10}		55			Y_{40}
26			Y_{11}		56			Y_{39}
27			Y_8		57			Y_{38}
28			Y_7		58			Y_{37}
29	V_{CC}				59			Y_{36}
30			Y_6		60			Y_{35}

(4) Diagram of HD44100 Package Dimentional Outline
(60-pin Plastic Flat Package)





(FP-60)

(Unit : mm)